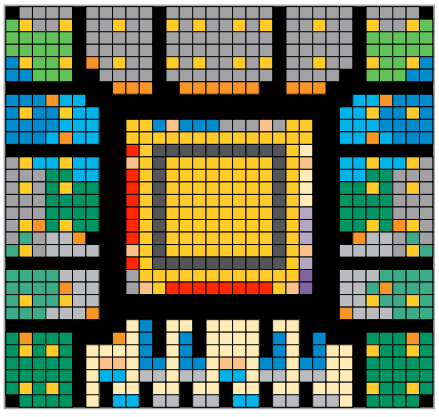
ECP5™ SERDES Enabled FPGA Family

Low-Cost, Low-Power, Small Form Factor

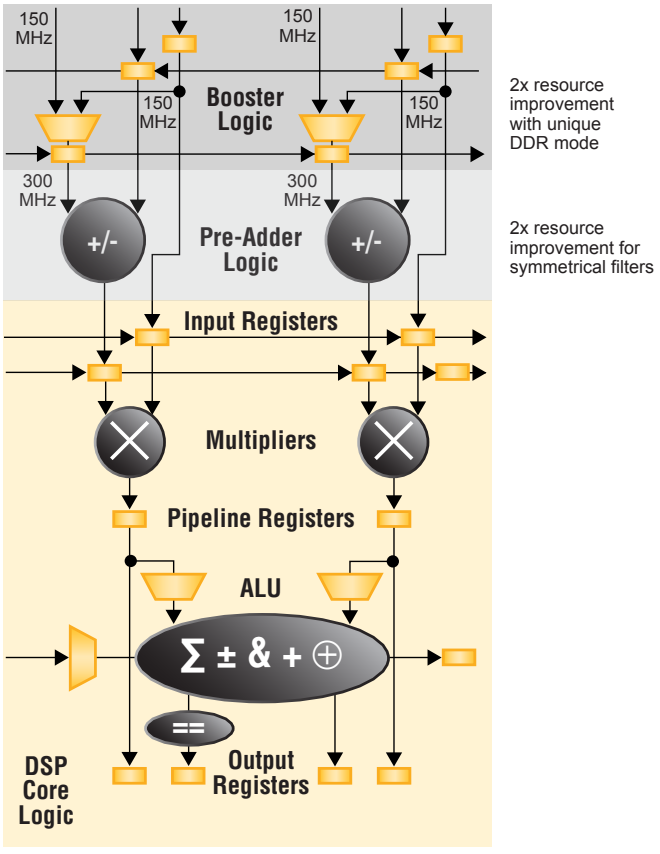
Designers of equipment for many emerging high volume applications are blending FPGAs with ASICs and ASSPs to rapidly build flexible systems that meet tight cost, power and form factor constraints. In developing the ECP5™ FPGA family, Lattice breaks the rule that all FPGAs should be the highest density, power hungry, and expensive. With a focus on compact, high volume applications, Lattice optimized the ECP5 architecture for low cost, small form factor and low power consumption. These characteristics make the ECP5 devices ideal for delivering programmable connectivity solutions to complement ASICs and ASSPs.

Key Features and Benefits

- **Cost Optimized Architecture**
  - Focused on providing best value below 100K LUTs.
  - Smart ball depopulation simplifies package integration with existing PCB technology.
  - Double Data Rate capability improves DSP block utilization.
- **Small Packages with High Functional Density**
  - 85K LUTs in 10x10 mm, 0.5 mm pitch package with SERDES.
- **Low Power Consumption**
  - Single channel SERDES functions below 0.25W.
  - Quad channel SERDES functions below 0.5W.



Smart ball depopulation
to simplify PCB routing



Enhanced sysDSP slices with
up to 4x resource improvement

Product Family Overview

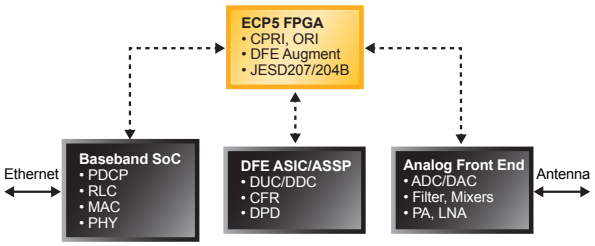
With up to 85K LUTs, 3.7Mbits embedded memory, 156 sysDSP blocks with DDR support, four 3.2Gbps SERDES channels and 365 user IO, the ECP5 devices provide a low-cost solution that meets the common connectivity requirements for complementing ASICs and ASSPs. A broad range of interface standards are supported including DDR3, LPDDR3, XGMII and 7:1 LVDS, PCI Express, Ethernet (XAUI, GbE, SGMII) and CPRI. The devices are offered in multiple package options with 1.1V core power supply, and also include support for encryption and dual boot capabilities. Smart depopulation of balls simplifies PCB board routing and reduces cost by utilizing fewer layers. Low power enhancements include stand-by mode operation of the individual blocks including SERDES, dynamic IO bank controllers and reduced operating voltage. The ECP5 family is supported by the Lattice Diamond™ design software, the leading-edge design and implementation tool optimized for cost sensitive, low-power Lattice FPGA architectures.

Device	LFE5UM-25	LFE5UM-45	LFE5UM-85	LFE5U-25	LFE5U-45	LFE5U-85
LUTs (K)	24	44	84	24	44	84
sysMEM Blocks (18 Kbits)	56	108	208	56	108	208
Embedded Memory (Kbits)	1,008	1,944	3,744	1,008	1,944	3,744
Distributed RAM Bits (Kbits)	194	351	669	194	351	669
18x18 Multipliers	28	72	156	28	72	156
SERDES (Dual/Channel)	1/2	2/4	2/4	0	0	0
PLLs/DLLs	2/2	4/4	4/4	2/2	4/4	4/4
Packages and SERDES Channels/I/O Combinations						
285 csfBGA (10x10 mm, 0.5 mm)	2/118	2/118	2/118	0/118	0/118	0/118
381 caBGA (17x17 mm, 0.8 mm)	2/197	4/203	4/205	0/197	0/203	0/205
554 caBGA (23x23 mm, 0.8 mm)		4/245	4/259		0/245	0/259
756 caBGA (27x27 mm, 0.8 mm)			4/365			0/365

End Market Application Examples

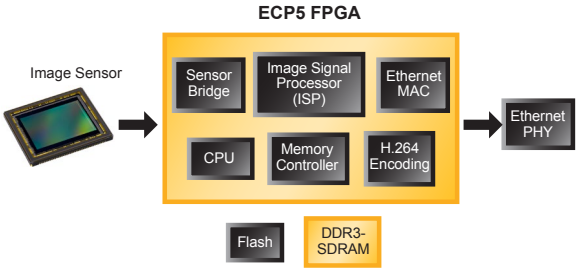
Low-Cost Connectivity for Small Cell Wireless Base Stations

- Flexible interfacing options to Digital Front End (DFE) including CPRI, ORI and compressed CPRI.
- DFE augment processing for pico cells such as multi-carrier DUC/DDC and CFR.
- Flexible interfacing options to analog front end including LVDS, JESD207, and JESD204B.



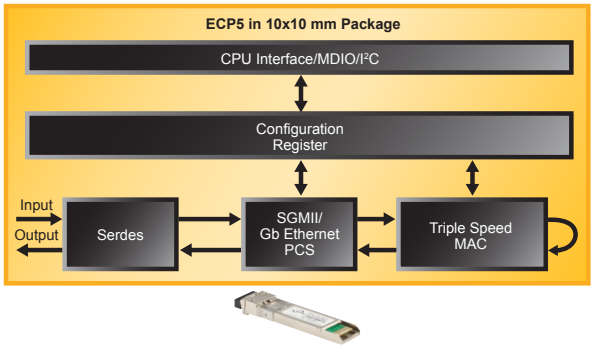
Low-Power Integration for Industrial Video Cameras

- Direct interfacing capability with single or multiple image sensors (MIPI CSI-2, sub-LVDS, HiSPi, Parallel).
- High-performance Wide Dynamic Range (WDR) and Image Signal Processing capabilities supported by Embedded Block RAM (EBR), and embedded DSP blocks.
- Flexible video interfacing options including integrated high-speed SERDES channels, LVDS, PCIe, and GigE.



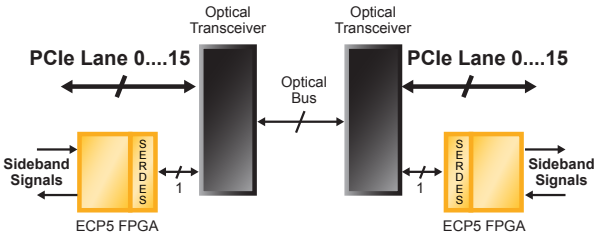
Small Form Factor Solution for Smart SFPs

- Smart SFP solution with integrated Operation and Maintainence (OAM) for remote control.
- ECP5 in 10x10 package enables small form factor solution for optical modules.
- SERDES and triple speed MAC for low-cost, low-power connectivity.



Low-Cost, Low-Power PCIe Side-Band Solution for Microservers

- Extract control plane data from I²C or SPI onto a high speed link such as PCIe.
- Implemented with low-power and size overhead PCIe sideband signaling.
- Leverage low-cost ECP5 SERDES, SGMII, and PCIe link layer solution.



Applications Support
techsupport@latticesemi.com

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