

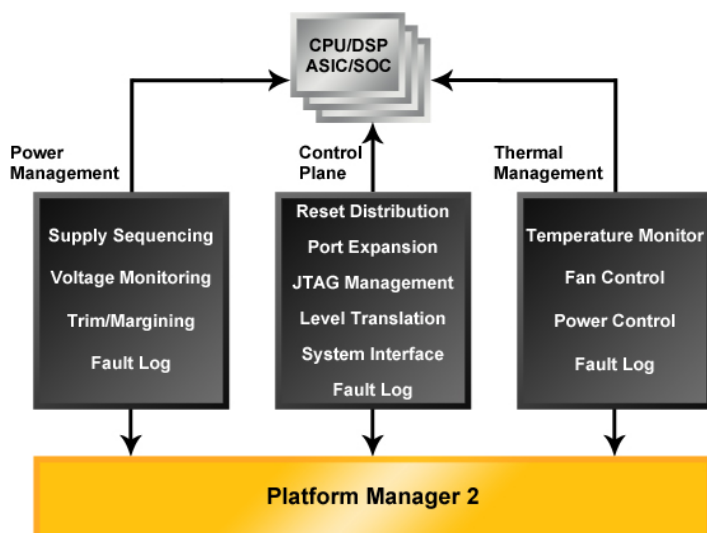
Platform Manager™ 2

Scalable Hardware Management Controller

Platform Manager™ 2 devices feature programmable analog with FPGA on a single chip to integrate all hardware management (power, thermal and control plane management) functions in a circuit board. The Platform Manager 2 architecture uses centrally located Hardware Management algorithm within the FPGA to control distributed hardware management expanders (L-ASC10 ICs) to integrate power, thermal and control plane management functions cost effectively from simple to complex boards

The Platform Designer™ tool integrated in Lattice Diamond software provides a single design environment to integrate a circuit board's hardware management using LogiBuilder (GUI based Logic entry), Verilog or VHDL. The correct-by-construction (automatic selection, customization and wiring of IPs for a given design) design methodology enables seamless scaling of analog channels, Digital I/O and FPGA LUTs to optimally meet specific hardware management requirements of a given board.

Power management functions include monitoring, supply sequencing, fault log, voltage scaling/VID control, trimming and margining functions. Thermal Management includes temperature monitoring, fan speed control, power control and fault log. The Control plane management include reset distribution, I2C/SPI port expansion, Level translation, System interface, fault logging, and other glue logic.



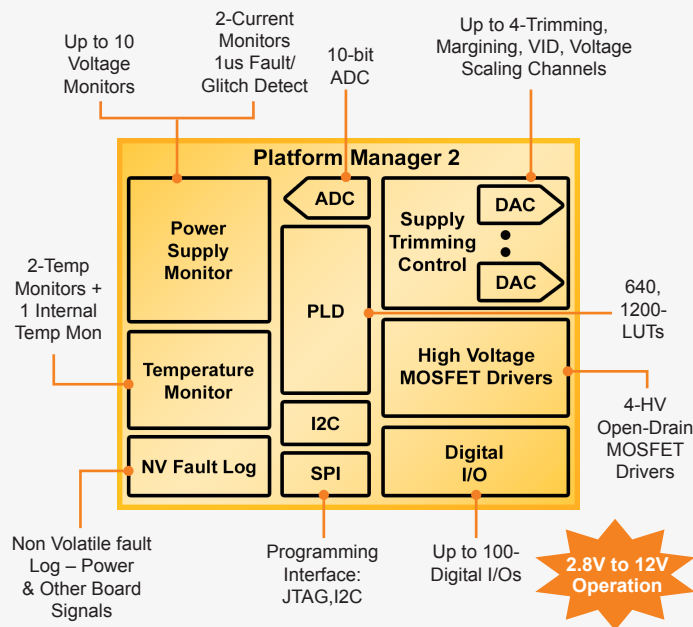
Increases Reliability	• Ample monitoring resources for full fault coverage • Accurate (0.2%) and Fast (<100us) Fault detection on any channel • Minimizes fault propagation through abundant communication between hardware management sub-blocks • Integrates power, thermal, control plane management algorithm into a single device
Reduces Time to Market	• Single design environment covers wide range of design complexities reducing design time • Fully verified hardware management through end-to-end simulation • Reduced design effort through correct-by-construction design methodology • Distributed sense and centralized control methodology minimizes circuit board layout congestion • Fault log, software based regression test support reduces board debug time
Lowens BOM and Cost	• Reduce BOM cost up to 50% versus multiple ICs • Needs fewer number of I/O in a CPLD • Reduced board area and layers saves additional cost
Reduces Risk	• Simulation reduces design errors before board layout • Re-programmability minimizes risk of board re-spins • Significantly reduces time-to-market

Key Features and Benefits

- **Optimized Hardware Management through Scalability**
 - 8 to 80 Precision Voltage Monitor Channels
 - 3 to 24 Temperature Monitoring Channels
 - 60 to 334 I/O and 640 to 6864 LUT Density
- **Precision Voltage Monitoring Increases Reliability**
 - Programmable Threshold from 0.67V to 5.7V & 4.5V to 13.2V
 - Differential input sensing
 - Over/under voltage detection with window comparison
 - 10-bit voltage measurement ADC
- **Temperature Monitoring Simplifies Thermal Management**
 - Measures Temperature using External Diode
 - Over/under temperature detection
 - Temperature Measurement range -60 to +150C
- **High-side current measurement reduces BOM**
 - Measures current across shunt resistor
 - Differential range 7.5mV to 200mV
 - Common mode voltage up to 13V
 - Programmable Gain amplifier for current measurement
 - Fast fault detection (1µs) and over current detection
- **High-Voltage FET Drivers Reduce # POLs needed**
 - Scalable from 4 to 32 N-channel MOSFET drivers
 - Digitally controlled power supply ramp control
 - Open drain output support
- **Margining and Trimming For Quality Assurance**
 - Scale from 4 to 32 power supplies
 - Digital closed-loop mode of operation
 - Voltage scaling and VID control
- **PLD to integrate power, thermal & control plane functions**
 - Up to 6864 LUT FPGA and up to 334 Digital I/O
 - Support for multiple interface standards
- **System Level Support**
 - Single 3.3V or 12V supply operation
 - Industrial temperature range
- **In-System Re-programmability Reduces Risk**
 - On-chip configuration memory
 - JTAG/I2C programming interface and background update
 - Dual-boot recovery

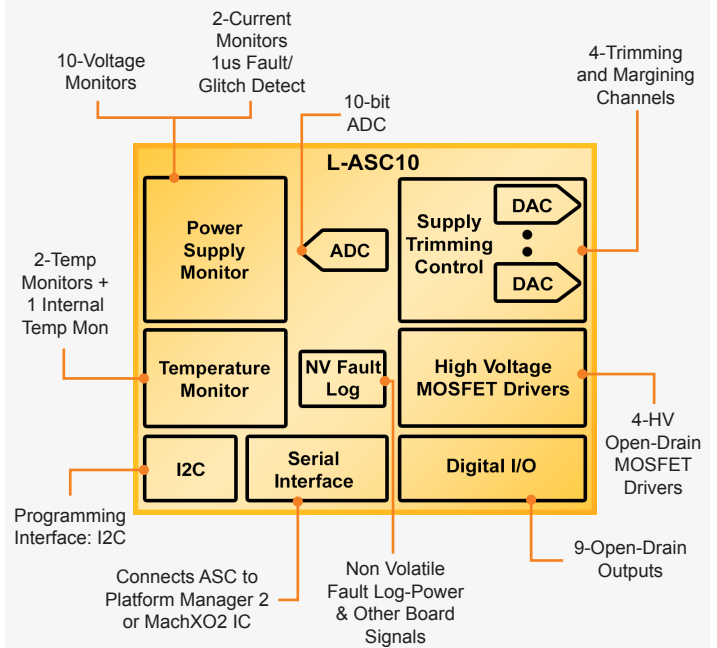
Platform Manager 2 Architecture

Hardware Management Controller

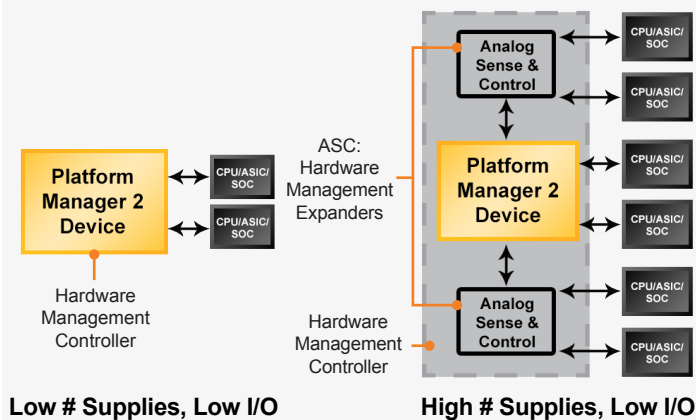


Analog Sense and Control (L-ASC10)

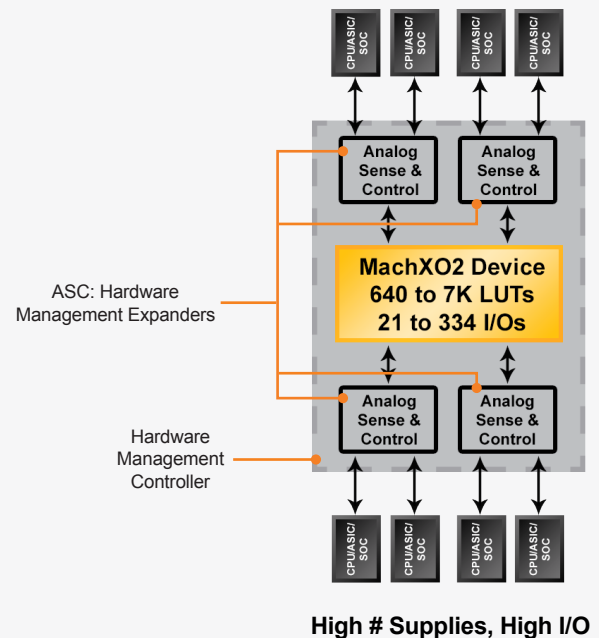
Hardware Management Expander



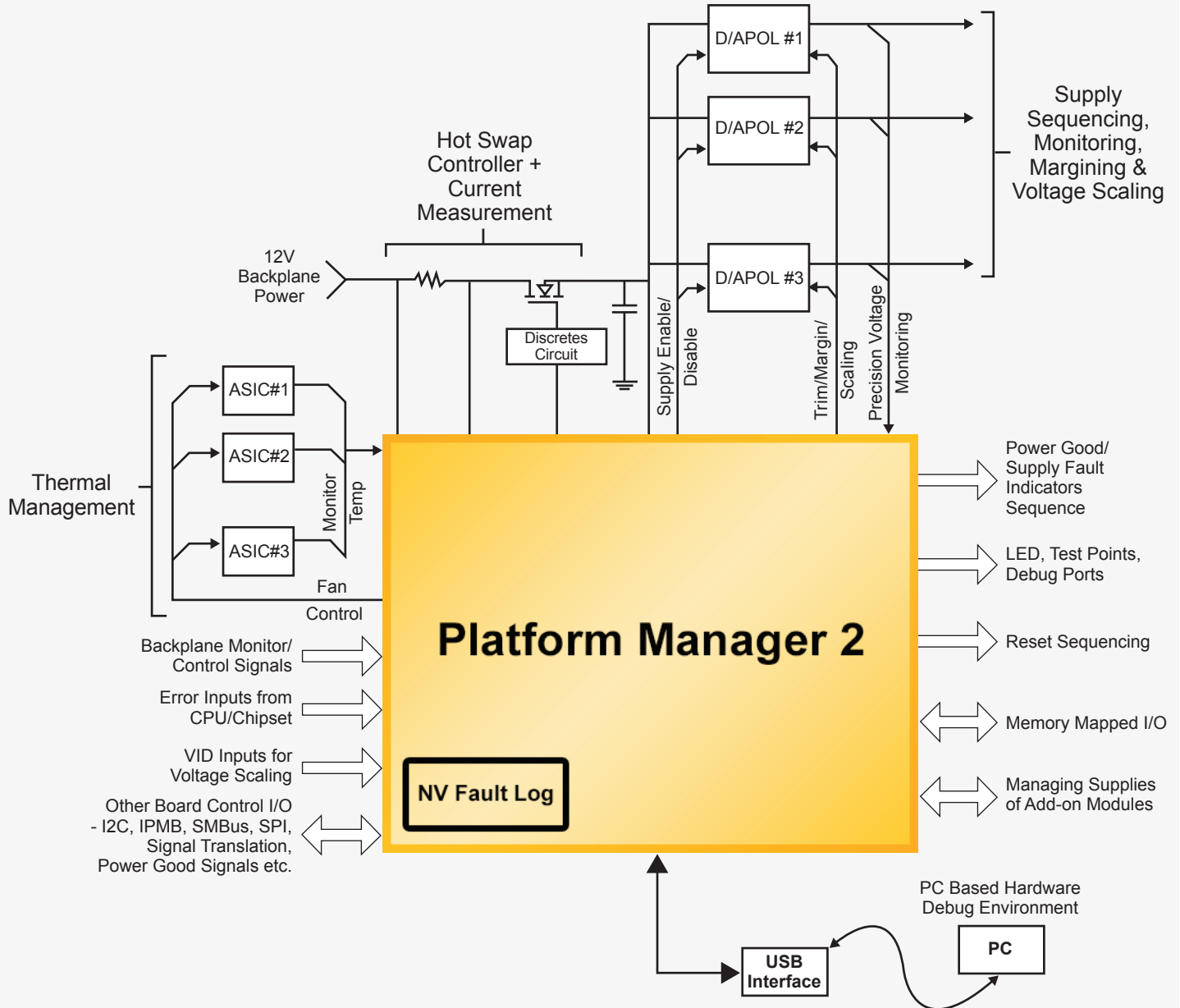
Hardware Management Using Platform Manager 2



Hardware Management Using MachXO2 + L-ASC10



Hardware Management With Platform Manager 2



Advantages

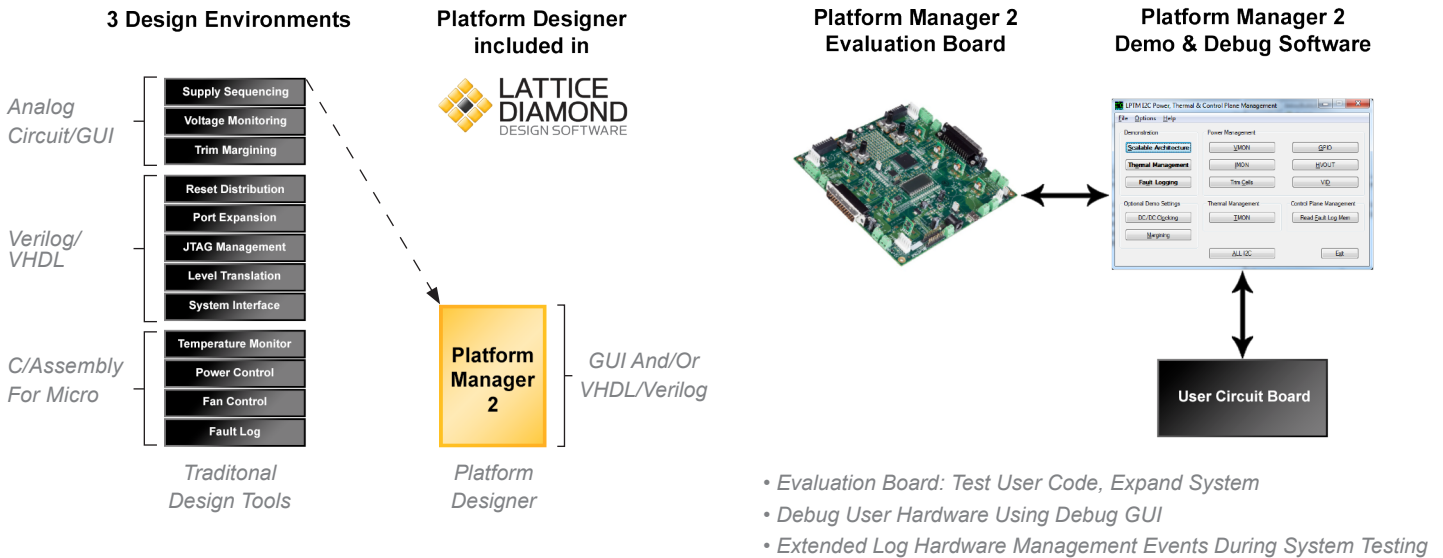
- Increased Reliability
- Smaller Board Space
- Reduced Number of Components
- Reduced Risk of Board Re-spin
- Reduced Time to Market
- Standard Solution Across a Wide Range of Applications
- Single Design Environment with End-to-end Simulation

Platform Designer

Unified, Flexible, Verifiable Design Methodology

Development Tools

Development Boards + Debug Aid Software



Platform Manager 2 Family

	H/W Management Expander	Hardware Management Controller	
	L-ASC10	LPTM20	LPTM21
Voltage Monitoring Inputs	10	8	10
Current Monitoring Inputs	2	2	2
Temperature Monitoring Inputs	2	2	2
Number of Trimming Channels	4	2	4
MOSFET Drives	4	4	4
On-Chip Non-Volatile Fault Log	✓	✓	✓
Number of LUTs	-	640	1280
Distributed RAM (Kbits)	-	5	10
EBR SRAM (kBits)	-	18	64
Number of EBR Blocks (9 kBits)	-	2	7
User Flash Memory (kBits)	-	24	64
Number of PLLs	-	0	1
Communication I/F	I2C	I2C/SPI/JTAG	
Programming Interface	I2C	I2C/SPI/JTAG	
Operating Voltage	3.3	2.8V to 12V	
Insystem Update Support	Yes		
Package Options	Digital I/Os		
48-pin QFN (7 X 7)	9		
128-pin TQFP (14X14)		60	
237-Ball ftBGA (1mm) (17X17)			106

Applications Support

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December 2013
Order #: I0236