CHANGE NOTIFICATION

Linear Technology Corporation
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June 28, 2013

Dear Sir/Madam: PCN# 062813

Subject: Notification of Change to LTC3612, LTC3614, LTC3615, LTC3616

Please be advised that Linear Technology Corporation has made minor changes to the LTC3612, LTC3614, LTC3615/-1 and LTC3616 family of monolithic synchronous buck converters. A minor mask revision was made to improve application robustness and efficiency at low switching frequencies. The original production silicon turns off the low side switch too early in some applications, which leads to current flow in the body diode. The revised silicon avoids this limitation and improves efficiency in low frequency (<600 KHz) Burst Mode operation. Further, the external Soft Start function was improved to keep the output voltage in regulation during fast drops in input voltage.

In addition, in order to improve manufacturability, the specification for the minimum top switch current limit at 100% duty cycle will be reduced slightly for the LTC3612, LTC3614 and LTC3616 as shown in the attached redlined specifications. The LTC3615/LTC3615-1 specifications and datasheet are unchanged.

These changes were qualified by performing characterization over the full operating junction temperature range and through rigorous engineering bench evaluations. In addition, each product successfully completed 1000 hours of HTOL stress. Product built using the new die and tested to the updated specification will be shipped with a datecode of approximately 1348.

Should you have any further questions, please feel free to contact me at 408-432-1900 ext. 2077, or by email at JASON.HU@LINEAR.COM. If I do not hear from you by August 29th, 2013, we will consider this change to be approved by your company.

Sincerely,

Jason Hu
Quality Assurance Engineer

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V, RT/SYNC = SV_{IN}, unless otherwise specified (Note 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage Range		●	2.25		5.5	V
V_{UVLO}	Undervoltage Lockout Threshold	SV_{IN} Ramping Down SV_{IN} Ramping Up	● ●	1.7		 2.25	V V
V_{FB}	Feedback Voltage Internal Reference	(Notes 3, 4) $V_{TRACK/SS}$ = SV_{IN}, V_{DDR} = 0V 0°C < T_J < 85°C –40°C < T_J < 125°C	 ●	 0.594 0.591	 0.6 	 0.606 0.609	 V V
	Feedback Voltage External Reference (Note 7)	(Notes 3, 4) $V_{TRACK/SS}$ = 0.3V, V_{DDR} = SV_{IN}		0.289	0.3	0.311	V
		(Notes 3, 4) $V_{TRACK/SS}$ = 0.5V, V_{DDR} = SV_{IN}		0.489	0.5	0.511	V
I_{FB}	Feedback Input Current	V_{FB} = 0.6V	●			±30	nA
$\Delta V_{LINEREG}$	Line Regulation	SV_{IN} = PV_{IN} = 2.25V to 5.5V (Notes 3, 4) TRACK/SS = SV_{IN}	●			0.2	%/V
$\Delta V_{LOADREG}$	Load Regulation	ITH from 0.5V to 0.9V (Notes 3, 4) V_{ITH} = SV_{IN} (Note 5)				0.25 2.6	% %
I_S	Active Mode	V_{FB} = 0.5V, V_{MODE} = SV_{IN} (Note 6)			1100		µA
	Sleep Mode	V_{FB} = 0.7V, V_{MODE} = 0V, ITH = SV_{IN} (Note 5)			70	100	µA
		V_{FB} = 0.7V, V_{MODE} = 0V (Note 4)			120	160	µA
	Shutdown	SV_{IN} = PV_{IN} = 5.5V, V_{RUN} = 0V			0.1	1	µA
$R_{DS(ON)}$	Top Switch On-Resistance	PV_{IN} = 3.3V (Note 10)			70		mΩ
	Bottom Switch On-Resistance	PV_{IN} = 3.3V (Note 10)			45		mΩ
I_{LIM}	Top Switch Current Limit	Sourcing (Note 8), V_{FB} = 0.5V Duty Cycle <35% Duty Cycle = 100%		5.2 ~~4~~ 3.7	6	6.8	A A
	Bottom Switch Current Limit	Sinking (Note 8), V_{FB} = 0.7V, Forced Continuous Mode		–3	–4	–5	A
$g_{m(EA)}$	Error Amplifier Transconductance	–5µA < I_{ITH} < 5µA (Note 4)			200		µS
I_{EAO}	Error Amplifier Max Output Current	(Note 4)			±30		µA
t_{SS}	Internal Soft-Start Time	V_{FB} from 0.06V to 0.54V, TRACK/SS = SV_{IN}		0.65	1	1.5	ms
$V_{TRACK/SS}$	Enable Internal Soft-Start	(Note 7)		0.62			V
t_{TRACK/SS_DIS}	Soft-Start Discharge Time at Start-Up			70			µs
$R_{ON(TRACK/SS\_DIS)}$	TRACK/SS Pull-Down Resistor at Start-Up					200	Ω
f_{OSC}	Oscillator Frequency	RT/SYNC = 370k	●	0.8	1	1.2	MHz
	Internal Oscillator Frequency	$V_{RT/SYNC}$ = SV_{IN}	●	1.8	2.25	2.7	MHz
f_{SYNC}	Synchronization Frequency			0.3		4	MHz
$V_{RT/SYNC}$	SYNC Level High			1.2			V
	SYNC Level Low			.		0.3	V
$I_{SW(LKG)}$	Switch Leakage Current	SV_{IN} = PV_{IN} = 5.5V, V_{RUN} = 0V			0.1	1	µA
V_{DDR}	DDR Option Enable Voltage			SV_{IN} – 0.3			V
V_{MODE} (Note 9)	Internal Burst Mode Operation					0.3	V
	Pulse-Skipping Mode			SV_{IN} – 0.3			V
	Forced Continuous Mode			1.1		SV_{IN} • 0.58	V
	External Burst Mode Operation			0.45		0.8	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V, RT/SYNC = SV_{IN} unless otherwise specified (Notes 1, 2, 11).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage Range		●	2.25		5.5	V
V_{UVLO}	Undervoltage Lockout Threshold	SV_{IN} Ramping Down SV_{IN} Ramping Up	● ●	1.7		 2.25	V V
V_{FB}	Feedback Voltage Internal Reference	(Note 3) V_{TRACK} = SV_{IN}, V_{DDR} = 0V 0°C < T_J < 85°C –40°C < T_J < 125°C	 ●	 0.594 0.591	 0.6	 0.606 0.609	 V V
	Feedback Voltage External Reference (Note 7)	(Note 3) V_{TRACK} = 0.3V, V_{DDR} = SV_{IN}		0.288	0.300	0.312	V
		(Note 3) V_{TRACK} = 0.5V, V_{DDR} = SV_{IN}		0.488	0.500	0.512	V
I_{FB}	Feedback Input Current	V_{FB} = 0.6V	●			±30	nA
$\Delta V_{LINEREG}$	Line Regulation	SV_{IN} = PV_{IN} = 2.25V to 5.5V (Notes 3, 4) TRACK/SS = SV_{IN}	●			0.2	%/V
$\Delta V_{LOADREG}$	Load Regulation	ITH from 0.5V to 0.8V (Notes 3, 4) V_{ITH} = SV_{IN} (Note 5)				0.25 2.6	% %
I_S	Active Mode Supply Current	V_{FB} = 0.5V, V_{MODE} = SV_{IN} (Note 6)			1100		µA
	Sleep Mode Supply Current	V_{FB} = 0.7V, V_{MODE} = 0V, ITH = SV_{IN} (Note 5)			75	100	µA
		V_{FB} = 0.7V, V_{MODE} = 0V (Note 4)			130	175	µA
	Shutdown Current	SV_{IN} = PV_{IN} = 5.5V, V_{RUN} = 0V			0.1	1	µA
$R_{DS(ON)}$	Top Switch On-Resistance	PV_{IN} = 3.3V (Note 10)			35		mΩ
	Bottom Switch On-Resistance	PV_{IN} = 3.3V (Note 10)			25		mΩ
I_{LIM}	Top Switch Current Limit	Sourcing (Note 8), V_{FB} = 0.5V Duty Cycle <35% Duty Cycle = 100%		7.5 ~~5.3~~ 5	9	10.5	A A
	Bottom Switch Current Limit	Sinking (Note 8), V_{FB} = 0.7V, Forced Continuous Mode		–6	–8	–11	A
$g_{m(EA)}$	Error Amplifier Transconductance	–5µA < I_{ITH} < 5µA (Note 4)			200		µS
I_{EAO}	Error Amplifier Maximum Output Current	(Note 4)			±30		µA
t_{SS}	Internal Soft-Start Time	V_{FB} from 0.06V to 0.54V, TRACK/SS = SV_{IN}		0.65	1.2	1.9	ms
$V_{TRACK/SS}$	Enable Internal Soft-Start	(Note 7)		0.62			V
t_{TRACK/SS_DIS}	Soft-Start Discharge Time at Start-Up			60			µs
$R_{ON(TRACK/SS\_DIS)}$	TRACK/SS Pull-Down Resistor at Start-Up					200	Ω
f_{OSC}	Oscillator Frequency	RT/SYNC = 370k	●	0.8	1	1.2	MHz
	Internal Oscillator Frequency	$V_{RT/SYNC}$ = SV_{IN}	●	1.8	2.25	2.7	MHz
f_{SYNC}	Synchronization Frequency Range			0.3		4	MHz
$V_{RT/SYNC}$	SYNC Input Threshold High			1.2			V
	SYNC Input Threshold Low			.		0.3	V
$I_{SW(LKG)}$	Switch Leakage Current	SV_{IN} = PV_{IN} = 5.5V, V_{RUN} = 0V			0.1	1	µA
V_{DDR}	DDR Option Enable Voltage			SV_{IN} – 0.3			V
V_{MODE} (Note 9)	Internal Burst Mode Operation					0.3	V
	Pulse-Skipping Mode			SV_{IN} – 0.3			V
	Forced Continuous Mode			1.1		SV_{IN} • 0.58	V
	External Burst Mode Operation			0.45		0.8	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 3.3V, RT/SYNC = SV_{IN} unless otherwise specified (Notes 1, 2, 11).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage Range		●	2.25		5.5	V
V_{UVLO}	Undervoltage Lockout Threshold	SV_{IN} Ramping Down SV_{IN} Ramping Up	● ●	1.7		 2.25	V V
V_{FB}	Feedback Voltage Internal Reference	(Note 3) V_{TRACK} = SV_{IN}, V_{DDR} = 0V 0°C < T_J < 85°C –40°C < T_J < 125°C	 ●	 0.594 0.591	 0.6	 0.606 0.609	 V V
	Feedback Voltage External Reference (Note 7)	(Note 3) V_{TRACK} = 0.3V, V_{DDR} = SV_{IN}		0.275	0.300	0.325	V
		(Note 3) V_{TRACK} = 0.5V, V_{DDR} = SV_{IN}		0.475	0.500	0.525	V
I_{FB}	Feedback Input Current	V_{FB} = 0.6V	●			±30	nA
$\Delta V_{LINEREG}$	Line Regulation	SV_{IN} = PV_{IN} = 2.25V to 5.5V (Notes 3, 4) TRACK/SS = SV_{IN}	●			0.2	%/V
$\Delta V_{LOADREG}$	Load Regulation	ITH from 0.5V to 0.9V (Notes 3, 4) V_{ITH} = SV_{IN} (Note 5)				0.25 2.6	% %
I_S	Active Mode	V_{FB} = 0.5V, V_{MODE} = SV_{IN} (Note 6)			1100		µA
	Sleep Mode	V_{FB} = 0.7V, V_{MODE} = 0V, ITH = SV_{IN} (Note 5)			75	100	µA
		V_{FB} = 0.7V, V_{MODE} = 0V (Note 4)			130	175	µA
	Shutdown	SV_{IN} = PV_{IN} = 5.5V, V_{RUN} = 0V			0.1	1	µA
$R_{DS(ON)}$	Top Switch On-Resistance	PV_{IN} = 3.3V (Note 10)			35		mΩ
	Bottom Switch On-Resistance	PV_{IN} = 3.3V (Note 10)			25		mΩ
I_{LIM}	Top Switch Current Limit	Sourcing (Note 8), V_{FB} = 0.5V Duty Cycle <35% Duty Cycle = 100%		 10.5 ~~8~~ 7.6	 12	 13.5	 A A
	Bottom Switch Current Limit	Sinking (Note 8), V_{FB} = 0.7V, Forced Continuous Mode		–6	–8	–11	A
$g_{m(EA)}$	Error Amplifier Transconductance	–5µA < I_{ITH} < 5µA (Note 4)			200		µS
I_{EAO}	Error Amplifier Maximum Output Current	(Note 4)			±30		µA
t_{SS}	Internal Soft-Start Time	V_{FB} from 0.06V to 0.54V, TRACK/SS = SV_{IN}		0.65	1.2	1.9	ms
$V_{TRACK/SS}$	Enable Internal Soft-Start	(Note 7)		0.62			V
t_{TRACK/SS_DIS}	Soft-Start Discharge Time at Start-Up			60			µs
$R_{ON(TRACK/SS\_DIS)}$	TRACK/SS Pull-Down Resistor at Start-Up					200	Ω
f_{OSC}	Oscillator Frequency	RT/SYNC = 370k	●	0.8	1	1.2	MHz
	Internal Oscillator Frequency	$V_{RT/SYNC}$ = SV_{IN}	●	1.8	2.25	2.7	MHz
f_{SYNC}	Synchronization Frequency Range			0.3		4	MHz
$V_{RT/SYNC}$	SYNC Level High			1.2			V
	SYNC Level Low			.		0.3	V
$I_{SW(LKG)}$	Switch Leakage Current	SV_{IN} = PV_{IN} = 5.5V, V_{RUN} = 0V			0.1	1	µA
V_{DDR}	DDR Option Enable Voltage			SV_{IN} – 0.3			V
V_{MODE} (Note 9)	Internal Burst Mode Operation					0.3	V
	Pulse-Skipping Mode			SV_{IN} – 0.3			V
	Forced Continuous Mode			1.1		SV_{IN} • 0.58	V
	External Burst Mode Operation			0.45		0.8	V