CHANGE NOTIFICATION

Linear Technology Corporation
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(408) 432-1900

July 21, 2014

Dear Sir/Madam: PCN# 072114

Subject: Notification of Change to LTC2482, LTC2483 Datasheet

Please be advised that Linear Technology Corporation has made a change to the LTC2482, LTC2483, specifications in order to improve device manufacturability. The Maximum External Oscillator Frequency (f_{EOSC}) in the Timing Characteristics is being reduced from 4000kHz to 1000kHz.
No changes are being made to the circuit or the test methodology. Product shipped after September 21, 2014 will be tested to the new limit.

Should you have any further questions, please feel free to contact me at 408-432-1900 ext. 2077, or by email at JASON.HU@LINEAR.COM. If I do not hear from you by September 21, 2014, we will consider this change to be approved by your company.

Sincerely,

Jason Hu
Quality Assurance Engineer

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	(Note 15)	●	10		~~4000~~ 1000	kHz
t_{HEO}	External Oscillator High Period		●	0.125		100	µs
t_{LEO}	External Oscillator Low Period		●	0.125		100	µs
t_{CONV_1}	Conversion Time	Simultaneous 50Hz/60Hz External Oscillator	● ●	144.1	146.9 41036/f_{EOSC} (in kHz)	149.9	ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 10) External Oscillator (Notes 10, 11)			38.4 f_{EOSC}/8		kHz kHz
D_{ISCK}	Internal SCK Duty Cycle	(Note 10)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 10)	●			4000	kHz
t_{LESCK}	External SCK Low Period	(Note 10)	●	125			ns
t_{HESCK}	External SCK High Period	(Note 10)	●	125			ns
t_{DOUT_ISCK}	Internal SCK 24-Bit Data Output Time	Internal Oscillator (Notes 10, 12) External Oscillator (Notes 10, 11)	● ●	0.61	0.625 192/f_{EOSC} (in kHz)	0.64	ms ms
t_{DOUT_ESCK}	External SCK 24-Bit Data Output Time	(Note 10)	●		24/f_{ESCK} (in kHz)		ms
t_1	$\overline{CS}$↓ to SDO Low		●	0		200	ns
t_2	CS↑ to SDO Hi-Z		●	0		200	ns
t_3	$\overline{CS}$↓ to SCKØ	(Note 10)	●	0		200	ns
t_4	$\overline{CS}$↓ to SCK≠	(Note 10)	●	50			ns
t_{KQMAX}	SCK↓ to SDO Valid		●			200	ns
t_{KQMIN}	SDO Hold After SCK↓	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS}$↓		●	50			ns
t_6	SCK Hold After $\overline{CS}$↓		●			50	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7V to 5.5V unless otherwise specified:

$V_{REFCM} = V_{REF}/2$, FS = $0.5V_{REF}$

$V_{IN} = IN^+ - IN^-$, $V_{IN(CM)} = (IN^+ + IN^-)/2$

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz rejection (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The SCK can be configured in external SCK mode or internal SCK mode. In external SCK mode, the SCK pin is used as digital input and the driving clock is f_{ESCK}. In internal SCK mode, the SCK pin is used as digital output and the output clock signal during the data output is f_{ISCK}.

Note 11: The external oscillator is connected to the f_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 12: The converter uses the internal oscillator.

Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: Guaranteed by design and test correlation.

Note 15: Refer to Applications Information section for performance vs data rate graphs.

Note 16: For V_{CC} < 3V, V_{IH} is 2.5V for pin f_O.

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range		●	10		~~4000~~1000	kHz
t_{HEO}	External Oscillator High Period		●	0.125		100	µs
t_{LEO}	External Oscillator Low Period		●	0.125		100	µs
t_{CONV_1}	Conversion Time	Simultaneous 50Hz/60Hz External Oscillator (Note 10)	● ●	144.1	146.9 41036/f_{EOSC}	149.9	ms ms

I²C TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 15)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(SDA)}$	Hold Time (Repeated) START Condition		●	0.6			µs
t_{LOW}	LOW Period of the SCL Clock Pin		●	1.3			µs
t_{HIGH}	HIGH Period of the SCL Clock Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated START Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time for Both SDA and SCL Signals	(Note 14)	●	20 + 0.1C_B		300	ns
t_f	Fall Time for Both SDA and SCL Signals	(Note 14)	●	20 + 0.1C_B		300	ns
$t_{SU(STO)}$	Set-Up Time for STOP Condition		●	0.6			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7V to 5.5V unless otherwise specified.

$V_{REF} = REF^+ – REF^–$, $V_{REFCM} = (REF^+ + REF^–)/2$, FS = 0.5$V_{REF}$;
$V_{IN} = IN^+ – IN^–$, $V_{INCM} = (IN^+ + IN^–)/2$.

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: 50Hz f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: 60Hz f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The external oscillator is connected to the CA0/F_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 11: The converter uses the internal oscillator.

Note 12: The output noise includes the contribution of the internal calibration operations.

Note 13: Guaranteed by design and test correlation.

Note 14: C_B = capacitance of one bus line in pF.

Note 15: All values refer to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.