# CHANGE NOTIFICATION

Linear Technology Corporation
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August 02, 2013

Dear Sir/Madam: PCN# 080213

**Subject: Notification of Change to LTC3411A Datasheet**

Please be advised that Linear Technology Corporation has made a minor change to the LTC3411A product datasheet to better center the parametric distribution within the specification range. The change is shown on the attached page of the marked up datasheet. There was no change made to the die. The product shipped after 10/04/2013 will be tested to the new limits.

Should you have any further questions, please feel free to contact me at 408-432-1900 ext. 2077, or by e-mail at JASON.HU@linear.com. If I do not hear from you by October 3st, 2013, we will consider this change approved by your company.

Sincerely,

Jason Hu
Quality Assurance Engineer

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_A$ = 25°C, $V_{IN}$ = 3.6V, $R_T$ = 125k unless otherwise specified. (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $I_S$ | Input DC Supply Current (Note 4)<br>Active Mode<br>Sleep Mode<br>Shutdown | <br>$V_{SYNC/MODE}$ = 3.6V, $V_{FB}$ = 0.75V<br>$V_{SYNC/MODE}$ = 3.6V, $V_{FB}$ = 0.84V<br>$V_{SHDN/RT}$ = 3.6V | | | <br>330<br>40<br>0.1 | <br>450<br>60<br>1 | <br>µA<br>µA<br>µA |
| $V_{SHDN/RT}$ | Shutdown Threshold High Active<br>Oscillator Resistor | | | | $V_{IN}$ – 0.6<br>125k | $V_{IN}$ – 0.4<br>1M | V<br>Ω |
| $f_{OSC}$ | Oscillator Frequency | $R_T$ = 125k<br>(Note 7) | | 2.25 | 2.5 | 2.8<br>4 | MHz<br>MHz |
| $f_{SYNC}$ | Synchronization Frequency | (Note 7) | | 0.4 | | 4 | MHz |
| $I_{LIM}$ | Peak Switch Current Limit | $V_{FB}$ = 0.5V | | 1.6 | 2.1 | 2.6 | A |
| $R_{DS(ON)}$ | Top Switch On-Resistance | MS Package<br>DD Package (Note 6) | | | 0.15<br>0.15 | 0.18 | Ω<br>Ω |
| | Bottom Switch On-Resistance | MS Package<br>DD Package (Note 6) | | | 0.13<br>0.13 | 0.16 | Ω<br>Ω |
| $I_{SW(LKG)}$ | Switch Leakage Current | $V_{IN}$ = 5.5V, $V_{SHDN/RT}$ = 5.5V, $V_{SW}$ = 0V or 5.5V | | | 0.01 | 1 | µA |
| $V_{UVLO}$ | Undervoltage Lockout Threshold | $V_{IN}$ Ramping Down | | 1.8 | 2.1 | 2.4 | V |
| PGOOD | Power Good Threshold | $V_{FB}$ Ramping Up from 0.68V to 0.8V<br>$V_{FB}$ Ramping Down from 0.92V to 0.8V | | –5<br>5 | –7<br>7 | | %<br>% |
| | Power Bad Threshold | $V_{FB}$ Ramping Down from 0.8V to 0.68V<br>$V_{FB}$ Ramping Up from 0.8V to 0.9V | | | –10<br>10 | –12<br>12 | %<br>% |
| $R_{PGOOD}$ | Power Good Pull-Down On-Resistance | | | | 15 | 30 | Ω |
| PGOOD Blanking | | $V_{FB}$ Step from 0V to 0.8V<br>$V_{FB}$ Step from 0.8V to 0V | | | 40<br>105 | | µs<br>µs |
| $V_{SYNC-MODE}$ | Pulse Skip<br>Force Continous<br>Burst | VIN = 2.5V to 5.5V<br>VIN = 2.5V to 5.5V<br>VIN = 2.5V to 5.5V | | 1.2<br>$V_{IN}$ – ~~0.75~~ | ~~1.1~~<br>0.6 | 0.6<br>~~0.63~~<br>$V_{IN}$ – ~~1.05~~ | 1.1 | V<br>V<br>V |
| $t_{SOFT-START}$ | | 10% to 90% of Regulation | | 0.5 | 0.8 | 1.0 | ms |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3411A is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3411AE is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3411AI is guaranteed over the full –40°C to 125°C operating junction temperature range. The maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

**Note 3:** The LTC3411A is tested in a feedback loop which servos $V_{FB}$ to the midpoint for the error amplifier ($V_{ITH}$ = 0.7V).

**Note 4:** Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

**Note 5:** $T_J$ is calculated from the ambient $T_A$ and power dissipation $P_D$ according to the following formulas:

LTC3411AEDD: $T_J = T_A + (P_D \bullet 43°C/W)$

LTC3411AEMS: $T_J = T_A + (P_D \bullet 120°C/W)$

**Note 6:** For the DD package, switch on-resistance is sampled at wafer level measurements and assured by design, characterization and correlation with statistical process controls.

**Note 7:** 4MHz operation is guaranteed by design but not production tested and is subject to duty cycle limitations (see Applications Information).

**Note 8:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.