

## CHANGE NOTIFICATION



Linear Technology Corporation  
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October 26, 2012

PCN#: 102612

Dear Sir/Madam:

**Subject:** Notification of Change to LTC1257 Datasheet

Please be advised that Linear Technology Corporation has made a minor change to the LTC1257 product datasheet to more accurately specify the Voltage Output Settling Time parameter. While auditing the LTC1257 test program in an effort toward continuous improvement LTC discovered an issue with the settling time specification. The hardware implementation for this test is not capable of repeatably and accurately measuring the settling time. We can no longer guarantee a maximum limit for this specification or guarantee this specification over temperature. The test will now be a typical specification with no temperature dot. The changes are shown on the marked up product datasheet pages as attached to this PCN. There was no change made to the die.

The product shipped after November 26th, 2012 will be tested to the new limits.

Should you have any further questions, please feel free to contact me at 408-432-1900 ext. 2519, or by e-mail at NGIRN@Linear.com. If I do not hear from you by November 26, 2012, we will consider this change to be approved by your company.

Sincerely,

Naib Girn  
Quality Assurance Manager

Confidential Statement  
This change notice is for Linear Technology's Customers only.  
Distribution or notification to third parties is prohibited

# New Data Sheet

LTC1257

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = T_{MIN}$  to  $T_{MAX}$ .  $V_{CC} = 4.75V$  to  $15.75V$ , internal or external reference ( $2.475V \leq V_{REF} \leq V_{CC} - 2.7V$ ), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OFF	Offset Error	When Using Internal Reference, LTC1257C	●			±8	LSB
		When Using Internal Reference, LTC1257I	●			±10	LSB
		When Using External Reference, LTC1257C	●			±4	mV
		When Using External Reference, LTC1257I	●			±5	mV
OFF <sub>TC</sub>	Offset Error Tempco	When Using Internal Reference (Note 2)	●		±0.02	±0.066	LSB/°C
		When Using External Reference (Note 2)	●		±15	±30	µV/°C
	Gain Error		●		0.5	±2	LSB
	Gain Error Tempco	(Note 2)	●		±0.01	±0.02	LSB/°C
Reference							
	Reference Output Voltage	I <sub>REF</sub> = 0, LTC1257C	●	2.028	2.048	2.068	V
		I <sub>REF</sub> = 0, LTC1257I	●	2.018		2.078	V
	Reference Output Tempco	I <sub>REF</sub> = 0	●		±0.06		LSB/°C
	Reference Line Regulation	I <sub>REF</sub> = 0, LTC1257C	●			±0.4	LSB/V
		I <sub>REF</sub> = 0, LTC1257I	●			±0.7	LSB/V
	Reference Load Regulation	0µA ≤ I <sub>REF</sub> ≤ 100µA	●			±1	LSB
	Reference Input Range	V <sub>CC</sub> > V <sub>REF</sub> + 2.7V	●	2.475		12	V
	Reference Input Resistance		●	8	14	18	kΩ
	Reference Input Capacitance	(Note 2)			15		pF
	Short-Circuit Current	V <sub>REF</sub> Shorted to GND	●			90	mA
Power Supply							
V <sub>CC</sub>	Positive Supply Voltage	For Specified Performance	●	4.75		15.75	V
I <sub>CC</sub>	Supply Current	4.75V ≤ V <sub>CC</sub> ≤ 5.25V	●		350	600	µA
		4.75V ≤ V <sub>CC</sub> ≤ 15.75V	●		800	1500	µA
Op Amp DC Performance							
	Short-Circuit Current Low	V <sub>OUT</sub> Shorted to GND	●			60	mA
	Short-Circuit Current High	V <sub>OUT</sub> Shorted to V <sub>CC</sub>	●			60	mA
	Output Impedance to GND	Input Code = 0	●		250	500	Ω
AC Performance							
	Voltage Output Slew Rate	5kΩ in Parallel with 100pF	●	1.0			V/µs
	Voltage Output Settling Time	To ±1/2LSB, 5kΩ in Parallel with 100pF, V <sub>CC</sub> = 4.75V			6		µs
	Digital Feedthrough	(Notes 2, 3)			50		nV/s
Digital I/O							
V <sub>IH</sub>	Digital Input High Voltage		●	2.4			V
V <sub>IL</sub>	Digital Input Low Voltage		●			0.8	V
V <sub>OH</sub>	Digital Output High Voltage	I <sub>OUT</sub> = -1mA, D <sub>OUT</sub> Only	●	V <sub>CC</sub> - 1			V
V <sub>OL</sub>	Digital Output Low Voltage	I <sub>OUT</sub> = 1mA, D <sub>OUT</sub> Only	●	0.4			V
I <sub>LEAK</sub>	Digital Input Leakage	V <sub>IN</sub> = GND to V <sub>CC</sub>	●			±10	µA
C <sub>IN</sub>	Digital Input Capacitance	(Note 2)	●			10	pF
Switching (Note 2)							
t <sub>1</sub>	D <sub>IN</sub> Valid to CLK Setup		●	100			ns
t <sub>2</sub>	D <sub>IN</sub> Valid to CLK Hold		●	25			ns
t <sub>3</sub>	CLK High Time		●	350			ns
t <sub>4</sub>	CLK Low Time		●	350			ns

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# Old Data Sheet

LTC1257

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = T_{MIN}$  to  $T_{MAX}$ .  $V_{CC} = 4.75V$  to  $15.75V$ , internal or external reference ( $2.475V \leq V_{REF} \leq V_{CC} - 2.7V$ ), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>Power Supply</b>							
$V_{CC}$	Positive Supply Voltage	For Specified Performance	●	4.75		15.75	V
$I_{CC}$	Supply Current	$4.75V \leq V_{CC} \leq 5.25V$ $4.75V \leq V_{CC} \leq 15.75V$	● ●		350 800	600 1500	$\mu A$ $\mu A$
<b>Op Amp DC Performance</b>							
	Short-Circuit Current Low	$V_{OUT}$ Shorted to GND	●			60	mA
	Short-Circuit Current High	$V_{OUT}$ Shorted to $V_{CC}$	●			60	mA
	Output Impedance to GND	Input Code = 0	●		250	500	$\Omega$
<b>AC Performance</b>							
	Voltage Output Slew Rate	$5k\Omega$ in Parallel with 100pF	●	1.0			V/ $\mu s$
	Voltage Output Settling Time	To $\pm 1/2LSB$ , $5k\Omega$ in Parallel with 100pF, $V_{CC} = 4.75V$	●			6	$\mu s$
	Digital Feedthrough	(Notes 2,3)			50		nV/s
<b>Digital I/O</b>							
$V_{IH}$	Digital Input High Voltage		●	2.4			V
$V_{IL}$	Digital Input Low Voltage		●			0.8	V
$V_{OH}$	Digital Output High Voltage	$I_{OUT} = -1mA$ , $D_{OUT}$ Only	●	$V_{CC} - 1$			V
$V_{OL}$	Digital Output Low Voltage	$I_{OUT} = 1mA$ , $D_{OUT}$ Only	●	0.4			V
$I_{LEAK}$	Digital Input Leakage	$V_{IN} = GND$ to $V_{CC}$	●			$\pm 10$	$\mu A$
$C_{IN}$	Digital Input Capacitance	(Note 2)	●			10	pF
<b>Switching (Note 2)</b>							
t1	$D_{IN}$ Valid to CLK Setup		●	100			ns
t2	$D_{IN}$ Valid to CLK Hold		●	25			ns
t3	CLK High Time		●	350			ns
t4	CLK Low Time		●	350			ns
t5	$\overline{LOAD}$ Pulse Width		●	150			ns
t6	LSB CLK to $\overline{LOAD}$		●	0			ns
t7	$\overline{LOAD}$ High to CLK		●	0			ns
t8	$D_{OUT}$ Output Delay	$C_{LOAD} = 15pF$	●	35		150	ns
f <sub>CLK</sub>	Maximum Clock Frequency					1.4	MHz