CHANGE NOTIFICATION

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900

November 07, 2011

PCN#: 110711

Dear Sir/Madam:

Subject: **Notification of Internal Die change for LTM2881**

Please be advised that Linear Technology Corporation has made a minor change to the LTM2881 internal die to eliminate an asynchronous event issue that can occur during short windows of certain time duration on the respective DI, A and B pins of this product. The time relationship of signal changes on these pins relative to other inputs or an internal refresh event could cause loss of information on the Y, Z or RO pins respectively. For current production silicon, the time window in which the problem occurs is very narrow for any single unit. However, when the problem occurs, a state change on Y, Z or RO will not occur as expected. For more details, please see the Product Errata document attached to this PCN.

The problem has been eliminated in the new silicon. The change has been fully characterized over the full operating temperature and voltage ranges and by performing op-life on 154 units at 125C for 1000 hrs.

No functional, parametric, mechanical, or datasheet specifications are affected, and the component bill of materials is unchanged. There are no changes associated with the package footprint, PCB layout or product top marking, so customer applications will be unaffected.

The product built using new die will be shipped with an approximate datecode of 1144.

Should you have any further questions, please feel free to contact me at 408-432-1900 ext. 2519, or by e-mail at Ngirn@Linear.com. If I do not hear from you by December 7th, 2011, we will consider this change to be approved by your company.

Sincerely,

Naib Girn
Quality Assurance Manager

Product Errata

LTM2881 Communication Issue

May 2011

Some LTM®2881 devices have an internal timing race condition that can cause signals passing through the isolation barrier to be delayed or inverted for up to one refresh period of 1.2µs ±0.15µs. This condition can occur if there is a specific narrow alignment of signal transitions and only if this is coincident with the rising edge of an internal asynchronous clock. Because of the tight alignment tolerance requirements and asynchronous nature of this event, this error is very infrequent. Workarounds are described in the following section. The LTM2881 is being revised to correct this issue. Contact Linear Technology Corporation regarding availability.

An example of an error is shown in Figure 1.

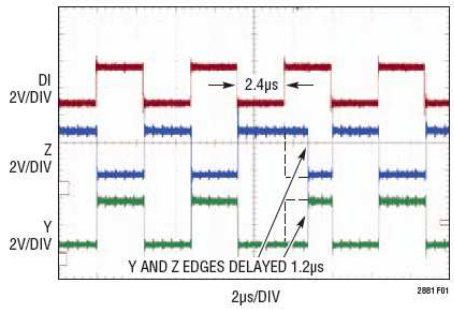

Figure 1. Error Example: DI Transitions Occur at Intervals That Are Multiples of 1.2µs, Causing the Y and Z Outputs to Be Delayed By 1.2µs

WORKAROUNDS

Most LTM2881 devices will never exhibit this behavior. However, to eliminate these errors in all devices, follow these guidelines:

Logic to Isolated Signaling

1. Switch DI so that transitions occur at intervals less than 1.05µs.
2. Do not change DE or TE 20ns ±5ns before a transition on DI.

If condition 1 cannot be met, then conditions A and B must be met:

A. Operate DI avoiding high and low times that are multiples of 1.2µs ±0.15µs.

B. Do not change DE or TE 1.2µs ±0.15µs, or multiples of this, before any transition on DI.

Isolated to Logic Signaling

3. Operate differential signal (A-B) avoiding high and low times that are multiples of 1.2µs ±0.15µs.
4. Maintain static input on pin D_{IN} when (A-B) is switching.

If condition 4 cannot be met, then conditions C and D must be met:

C. Do not change D_{IN} 40ns ±20ns after a transition on (A-B).

D. Do not change D_{IN} 1.2µs ±0.25µs, or multiples of this, before any transition on (A-B).

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT 0511 • PRINTED IN USA