CHANGE NOTIFICATION

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900

November 08, 2011

PCN#: 110811

Dear Sir/Madam:

Subject: **Notification of Internal Die change for LTM2882**

Please be advised that Linear Technology Corporation has made a minor change to the LTM2882 internal die to eliminate an asynchronous event issue that can occur during short windows of certain time duration on the respective T1IN and R1IN pins of this product. The time relationship of signal changes on these pins relative to other inputs or an internal refresh event could cause a loss of information on the T1OUT or R1OUT pins respectively. For current production silicon, the time window in which the problem occurs is very narrow for any single unit. However, when the problem occurs, a state change on T1OUT or R1OUT will not occur as expected. For more details, please see the Product Errata document attached to this PCN.

The problem has been eliminated in the new silicon. The change has been fully characterized over the full operating temperature and voltage ranges and by performing op-life on 154 units at 125C for 1000 hrs.

No functional, parametric, mechanical, or datasheet specifications are affected, and the component bill of materials is unchanged. There are no changes associated with the package footprint, PCB layout or product top marking, so customer applications will be unaffected.

The product built using new die will be shipped with an approximate datecode of 1144.

Should you have any further questions, please feel free to contact me at 408-432-1900 ext. 2519, or by e-mail at Ngirn@Linear.com. If I do not hear from you by December 8th, 2011, we will consider this change to be approved by your company.

Sincerely,

Naib Girn
Quality Assurance Manager

Product Errata

LTM2882 Communication Issue

May 2011

Some LTM®2882 devices have an internal timing race condition that can cause signals passing through the isolation barrier to be delayed or inverted for up to one refresh period of 1.2µs ±0.15µs. This condition can occur if there is a specific narrow alignment of signal transitions and only if this is coincident with the rising edge of an internal asynchronous clock. Because of the tight alignment tolerance requirements and asynchronous nature of this event, this error is very infrequent. Workarounds are described below. The LTM2882 is being revised to correct this issue. Contact Linear Technology Corporation regarding availability.

An example of an error is shown in Figure 1.

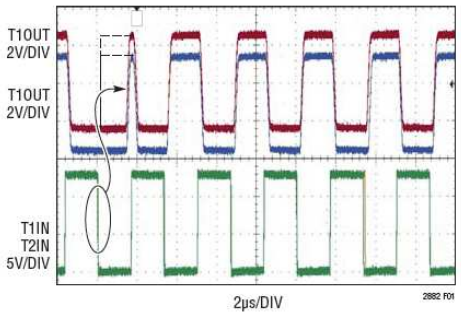

Figure 1. Error Example: T2IN Changes 20ns Before T1IN (On This Time Scale, T1IN and T2IN Appear to Be Coincident) Causing the T1OUT and T2OUT to Be Delayed By 1.2µs

WORKAROUNDS

Most LTM2882 devices will never exhibit this behavior. However, to eliminate these errors in all devices, follow these guidelines:

Logic to Isolated Signaling

1. Operate T1IN avoiding high and low times that are multiples of 1.2µs ±0.15µs.
2. Do not change T2IN or DIN 20ns ±5ns before a transition on T1IN.
3. Do not change T2IN or DIN 1.2µs ±0.15µs, or multiples of this, before any transition on T1IN.

Isolated to Logic Signaling

4. Operate R1IN avoiding high and low times that are multiples of 1.2µs ±0.18µs.
5. Do not change R2IN 20ns ±50ns before a transition on R1IN.
6. Do not change R2IN 1.2µs ±0.2µs, or multiples of this, before any transition on R1IN.

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