November 25, 2019

Subject: PCN#10A-19 Notification of Changes to CrossLink™ Data Sheet and CrossLink™ Automotive Data Sheet

Dear Lattice Customer,

Lattice Semiconductor is providing this notification of changes to the CrossLink Family Data Sheet (FPGA-DS-02007) and CrossLink Automotive Family Data Sheet (FPGA-DS-02013).

Change Description

CrossLink Family Data Sheet Changes:
The new CrossLink Family Data Sheet (FPGA-DS-02007 version 1.6 dated September 2019) includes updates to the following parameters:

Table 4.9. sysIO Single-Ended DC Electrical Characterizations

Parameter	Description	Version 1.5		Version 1.6	
		Min	Max	Min	Max
V_{IH}	LVCMOS18 Input High Voltage	0.65 V_{CCIO}	---	0.67 V_{CCIO}	---

Table 4.13. CrossLink External Switching Characteristics

Description	Version 1.5	Version 1.6
Generic SDR Interface	Present	Removed

Table 4.13. CrossLink External Switching Characteristics General Purpose I/O MIPI D-PHY Rx with 1:8 or 1:16 Gearing					
Parameter	**Description**	**Version 1.5**		**Version 1.6**	
		Conditions	**Min**	**Conditions**	**Min**
$t_{SU\_GDDRX\_MP}$	Input Data Set-Up Before CLK	900 Mb/s < Data Rate ≤ 1.20 Gb/s and V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.200	842 Mb/s < Data Rate ≤ 1.20 Gb/s and V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.200
		600 Mb/s < Data Rate ≤ 900 Mb/s and V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.150	473 Mb/s < Data Rate ≤ 842 Mb/s and V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.150
		Data Rate ≤ 600 Mb/s and V_{IDTH} = 70 mV V_{IDTL} = -70 mV	0.150	Data Rate ≤ 473 Mb/s and V_{IDTH} = 70 mV V_{IDTL} = -70 mV	0.150
$t_{HO\_GDDRX\_MP}$	Input Data Hold After CLK	900 Mb/s < Data Rate ≤ 1.20 Gb/s and V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.200	842 Mb/s < Data Rate ≤ 1.20 Gb/s and V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.200
		600 Mb/s < Data Rate ≤ 900 Mb/s and V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.150	473 Mb/s < Data Rate ≤ 842 Mb/s and V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.150
		Data Rate ≤ 600 Mb/s and V_{IDTH} = 70 mV V_{IDTL} = -70 mV	0.150	Data Rate ≤ 473 Mb/s and V_{IDTH} = 70 mV V_{IDTL} = -70 mV	0.150

Table 4.15. 1500 Mb/s MIPI_DPHY_X8_RX/TX Timing Table (1500 Mb/s > MIPI D-PHY Data Rate > 1200 Mb/s)					
Parameter	**Description**	**Version 1.5**		**Version 1.6**	
		Min	**Max**	**Min**	**Max**
t_{SU_MIPIX8}	Input Data Setup before CLK	0.200 UI	---	0.227 UI	---
t_{HO_MIPIX8}	Input Data Hold after CLK	0.200 UI	---	0.305 UI	---
t_{DVB_MIPIX8}	Output Data Valid before CLK Output	0.300 UI	---	0.200 UI	---
t_{DVA_MIPIX8}	Output Data Valid after CLK Output	0.300 UI	---	0.200 UI	---

Table 4.16. 1200 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1200 Mb/s > MIPI D-PHY Data Rate > 1000 Mb/s)					
Parameter	**Description**	**Version 1.5**		**Version 1.6**	
		Min	**Max**	**Min**	**Max**
t_{DVB_MIPIX4}	Output Data Valid before CLK Output	0.300 UI	---	0.200 UI	---
t_{DVA_MIPIX4}	Output Data Valid after CLK Output	0.300 UI	---	0.200 UI	---

Table 4.17. 1000 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1000 Mb/s > MIPI D-PHY Data Rate > 10 Mb/s)					
Parameter	**Description**	**Version 1.5**		**Version 1.6**	
		Min	**Max**	**Min**	**Max**
t_{DVB_MIPIX4}	Output Data Valid before CLK Output	0.350 UI	---	0.150 UI	---
t_{DVA_MIPIX4}	Output Data Valid after CLK Output	0.350 UI	---	0.150 UI	---

Table 4.20. CrossLink Automotive sysCONFIG Port Timing Specifications					
Parameter	**Description**	**Version 1.5**		**Version 1.6**	
		Min	**Max**	**Min**	**Max**
t_{PRGM}	Minimum CRESETB LOW pulse width required to restart configuration (from falling edge to rising edge)	145 ns	---	290 ns	---

See the data sheet revision history for other clarifications and changes.

There will be no changes to Diamond® 3.11 Software relating to this data sheet change.

CrossLink Automotive Family Data Sheet Changes:

The new CrossLink Automotive Family Data Sheet (FPGA-DS-02013 version 1.6 dated September 2019) includes updates to the following parameters:

Table 4.9. sysIO Single-Ended DC Electrical Characterizations					
Parameter	**Description**	**Version 1.5**		**Version 1.6**	
		Min	**Max**	**Min**	**Max**
V_{IH}	LVCMOS18 Input High Voltage	0.67 V_{CCIO}	---	0.68 V_{CCIO}	---

Table 4.10. LVDS/subLVDS/SLVS200					
Parameter	**Description**	**Version 1.5**		**Version 1.6**	
		Min	**Max**	**Min**	**Max**
V_{OS}	Output Voltage Offset (Common Mode Voltage)	1.125 V	1.375 V	1.080 V	1.400 V

Table 4.12. CrossLink Automotive Maximum I/O Buffer Speed		
Description	**Version 1.5**	**Version 1.6**
	Max	**Max**
MIPI D-PHY (HS Mode)	600 MHz	535 MHz
SLVS200, V_{CCIO} = 2.5 V	600 MHz	535 MHz

Table 4.13. CrossLink Automotive External Switching Characteristics		
Description	**Version 1.5**	**Version 1.6**
Generic SDR Interface	Present	Removed

Table 4.13. CrossLink Automotive External Switching Characteristics General Purpose I/O MIPI D-PHY Rx with 1:8 or 1:16 Gearing					
Parameter	**Description**	**Version 1.5**		**Version 1.6**	
		Conditions	**Min**	**Conditions**	**Min**
$t_{SU\_GDDRX\_MP}$	Input Data Set-Up Before CLK	900 Mb/s < Data Rate ≤ 1.2 Gb/s and V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.200	900 Mb/s < Data Rate ≤ 1.07 Gb/s and V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.200
		---	---	870 Mb/s < Data Rate ≤ 900 Mb/s and V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.160
		600 Mb/s < Data Rate ≤ 900 Mb/s and V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.150	450 Mb/s < Data Rate ≤ 870 Mb/s and V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.150
		Data Rate ≤ 600 Mb/s and V_{IDTH} = 70 mV V_{IDTL} = -70 mV	0.150	Data Rate ≤ 450 Mb/s and V_{IDTH} = 70 mV V_{IDTL} = -70 mV	0.150
$t_{HO\_GDDRX\_MP}$	Input Data Hold After CLK	900 Mb/s < Data Rate ≤ 1.2 Gb/s and V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.200	900 Mb/s < Data Rate ≤ 1.07 Gb/s and V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.200
		---	---	870 Mb/s < Data Rate ≤ 900 Mb/s and V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.160
		600 Mb/s < Data Rate ≤ 900 Mb/s and V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.150	450 Mb/s < Data Rate ≤ 870 Mb/s and V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.150
		Data Rate ≤ 600 Mb/s and V_{IDTH} = 70 mV V_{IDTL} = -70 mV	0.150	Data Rate ≤ 450 Mb/s and V_{IDTH} = 70 mV V_{IDTL} = -70 mV	0.150

Table 4.15. 1500 Mb/s MIPI_DPHY_X8_RX/TX Timing Table (1500 Mb/s > MIPI D-PHY Data Rate > 1200 Mb/s)					
Parameter	**Description**	**Version 1.5**		**Version 1.6**	
		Min	**Max**	**Min**	**Max**
t_{SU_MIPIX8}	Input Data Setup before CLK	0.200 UI	---	0.227 UI	---
t_{HO_MIPIX8}	Input Data Hold after CLK	0.200 UI	---	0.305 UI	---
t_{DVB_MIPIX8}	Output Data Valid before CLK Output	0.300 UI	---	0.200 UI	---
t_{DVA_MIPIX8}	Output Data Valid after CLK Output	0.300 UI	---	0.200 UI	---

Table 4.16. 1200 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1200 Mb/s > MIPI D-PHY Data Rate > 1000 Mb/s)					
Parameter	**Description**	**Version 1.5**		**Version 1.6**	
		Min	**Max**	**Min**	**Max**
t_{DVB_MIPIX4}	Output Data Valid before CLK Output	0.300 UI	---	0.200 UI	---
t_{DVA_MIPIX4}	Output Data Valid after CLK Output	0.300 UI	---	0.200 UI	---

Table 4.17. 1000 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1000 Mb/s > MIPI D-PHY Data Rate > 10 Mb/s)					
Parameter	**Description**	**Version 1.5**		**Version 1.6**	
		Min	**Max**	**Min**	**Max**
t_{DVB_MIPIX4}	Output Data Valid before CLK Output	0.350 UI	---	0.150 UI	---
t_{DVA_MIPIX4}	Output Data Valid after CLK Output	0.350 UI	---	0.150 UI	---

Table 4.20. CrossLink Automotive sysCONFIG Port Timing Specifications					
Parameter	**Description**	**Version 1.5**		**Version 1.6**	
		Min	**Max**	**Min**	**Max**
t_{PRGM}	Minimum CRESETB LOW pulse width required to restart configuration (from falling edge to rising edge)	145 ns	---	290 ns	---

See the data sheet revision history for other clarifications and changes.

There will be no changes to Diamond® 3.11 Software relating to this data sheet change.

Affected Products

The Ordering Part Numbers (OPNs) affected by the CrossLink Family Data Sheet changes are as follows:

LIF-MD6000-6UWG36ITR

LIF-MD6000-6UMG64I

LIF-MD6000-6MG81I

LIF-MD6000-6JMG80I

LIF-MD6000-6KMG80I

The Ordering Part Numbers (OPNs) affected by the CrossLink Automotive Family Data Sheet changes are as follows:

LIA-MD6000-6MG81E

LIA-MD6000-6JMG80E

LIA-MD6000-6KMG80E

Note: This PCN also affects all package, grade and tape/reel options and any custom devices (i.e. factory programmed, special test, etc.) which are derived from any of the devices listed above.

Datasheet Specifications

The updated CrossLink Family Data Sheet (FPGA-DS-02007 version 1.6 dated September 2019) and CrossLink Automotive Family Data Sheet (FPGA-DS-02013 version 1.6 dated September 2019) with the above changes are available on the Lattice website. The datasheet updates do not require bitstream changes.

Recommended Action

Table 4.9 V_{IH}: This change is only applicable to designs using CrossLink's Programmable I/Os as LVCMOS18 inputs. For these cases, customers should review their design to ensure the 1.8 V driver's V_{OH} level to CrossLink can meet the new minimum level.

Table 4.10 V_{OS} (Automotive FPGA-DS-02013 Only): This change is only applicable to designs using CrossLink's Programmable I/Os as LVDS transmitter. Customers should ensure that the LVDS receiver's input common mode voltage is within the expanded V_{OS} range.

Table 4.12 I/O Buffer Speed (Automotive FPGA-DS-02013 Only): This change is only applicable to designs using CrossLink's Programmable I/Os as MIPI D-PHY receiver or SLVS200 receiver. The change reduces the maximum line rate supported from 1.2 Gbps (600 MHz) to 1.07 Gbps (535 MHz). Customers need to ensure the MIPI/SLVS200 source does not exceed the new limit. Otherwise, a reduction in the design's line rate will be needed.

Table 4.13 SDR: This section of the table was informational only and has been removed from the data sheet. A design needs to run through the static timing analysis tool, TRACE, in Diamond® Software to ensure it achieves timing closure. If the design had previously achieved timing closure, no action is required.

Table 4.13 $t_{SU\_GDDRX\_MP}$ & $t_{HO\_GDDRX\_MP}$: The setup & hold time changes are only applicable when the Programmable I/Os are a configured as MIPI D-PHY receiver. The following table shows the MIPI D-PHY parameters and the values for conformance to the MIPI D-PHY Specification.

Symbol	Parameter	Min	Max	Unit
$T_{SETUP[RX]}$ / $t_{SU\_GDDRX\_MP}$	Data to Clock Setup Time (Rx), ≤ 1 Gbps	0.15	---	UI
$T_{SETUP[RX]}$ / $t_{SU\_GDDRX\_MP}$	Data to Clock Setup Time (Rx), > 1 Gbps	0.20	---	UI
$T_{HOLD[RX]}$ / $t_{HO\_GDDRX\_MP}$	Clock to Data Hold Time (Rx), ≤ 1 Gbps	0.15	---	UI
$T_{HOLD[RX]}$ / $t_{HO\_GDDRX\_MP}$	Clock to Data Hold Time (Rx), > 1 Gbps	0.20	---	UI
V_{IDTH}	Differential Input High Threshold	---	70	mV
V_{IDTL}	Differential Input Low Threshold	-70	---	mV

Depending on the data rate, Crosslink will require addition setup/hold time and/or increase threshold voltage. Customer needs to ensure the MIPI D-PHY transmitter meets the requirements outlined in Table 4.13.

Tables 4.15 t_{SU_MIPIX8} & t_{HO_MIPIX8}: The setup & hold time changes are only applicable when the Hardened MIPI D-PHY is being utilized, configured as MIPI D-PHY receiver and data rate is between 1200 Mbps to 1500 Mbps. Under these conditions, CrossLink will require additional setup & hold time than what is definited in the MIPI D-PHY Specification. Customer needs to ensure the MIPI D-PHY transmitter meets the requirements outlined in Table 4.15.

Table 4.15/4.16/4.17 t_{DVB_MIPIX8}, t_{DVA_MIPIX8}, t_{DVB_MIPIX4} & t_{BVA_MIPIX4}: The output data valid time changes are only applicable when the Hardened MIPI D-PHY is being utilized & configured as MIPI D-PHY transmitter. Customer needs to ensure the downstream MIPI D-PHY receiver can capture the data with the updated data valid times.

Table 4.20 t_{PRGM}: Customers need to ensure the external device that controls the CRESETB timing meets the new t_{PRGM} parameter value. Not meeting the new minimum pulse width may cause CrossLink to stay in User Mode and not re-start configuration.

Customers who have further questions regarding these changes are encouraged to contact local field support or at sales@latticesemi.com.

PCN Timing

The datasheet changes are effective immediately and retroactively. There are no changes to the devices, therefore samples are not applicable to these data sheet changes.

Lattice PCNs are available on the Lattice website. Please sign up to receive e-mail PCN alerts by registering here. If you already have a Lattice web account and wish to receive PCN alerts, you can do so by logging into your account and making edits to your subscription options.

Sincerely,

Lattice PCN Administration