



DATASHEET COMPARISON

Migrating from FM25V02-G to CY15B256Q-SXA	Parameter	FM25V02 (Old Part)	CY15B256Q (New Part)	Comments
	Reserved opcode	No specified	11000011b 11000010b 01011010b 01011011b	No change. These reserved opcodes do exist in the FM25V02-G parts but were not shown in the datasheet.
	Device ID	7F7F7F7F7FC22200h	7F7F7F7F7FC22288h	A system software update is required to update the device ID when migrating to the FM25V02A-G.
	Electrostatic discharge voltage (Human Body Model)	1000 V	2000 V	Improvement in the CY15B256Q-SXA part but no impact at the system level.
	Electrostatic discharge voltage (Charged Device Model)	1250 V	500 V	These are at the component level ESD specifications and do not have any impact on the system level ESD.
	Electrostatic discharge voltage (Machine Model)	200	Not provided	JEDEC has discontinued use of the Machine Model (MM) because the MM is redundant to HBM at the device level. Cypress follows JEDEC standard ESD qualification, therefore the Machine Model ESD specification is not provided.
	Input resistance (/HOLD pin), for VIN = VIH (min)	40 kΩ	30 kΩ	The CY15B256Q-SXA internal pull-up resistor on the /HOLD pin is ~20% stronger. This provides better noise immunity. However, this reduction in the resistor value increases the leakage current by ~20%.
	Input resistance (/HOLD pin), for VIN = VIL (max)	1000 kΩ	800 kΩ	
	Clock HIGH time (tCH) for SCK = 25 MHz	20 ns	18 ns	This is an improvement in the CY15B256Q-SXA part. This allows the master SPI clock (SCK) duty cycle variations in the range of 45% to 55%.
	Clock LOW time (tCL) for SCK = 25 MHz	20 ns	18 ns	
	Output data valid time (tODV)	18 ns	16 ns	This is an improvement in the CY15B256Q-SXA part. Data at the output will be available 2 ns earlier hence using CY15B256Q-SXA provides more setup time for the host controller data input pin.
	Power-up VDD (min) to first access (/CS LOW)	250 μs	1000 μs	If the system boots up faster than 1000 μs, this difference needs to be adjusted to meet power up to first access time for CY15B256Q-SXA. If the system boots up slower than 1000 μs, this difference doesn't trigger any change.

Migrating from FM24V02-G to CY15B256J-SXA	Parameter	FM24V02 (Old Part)	CY15B256J (New Part)	Comments
	Device ID	004200h	004221h	If the device ID is used then the system firmware/software will require update.
	Surface mount lead soldering temperature	260 °C for 10 seconds	260 °C for 3 seconds	The surface mount lead soldering temperature of 260 °C for 3 seconds allows up to three reflow cycles. Therefore, the soldering spec of both devices are the same, but stated differently. Refer to the following website for more details: http://www.cypress.com/?docID=29889
	Electrostatic discharge voltage (Human Body Model)	3500 V	2000 V	No impact at the system level.
	Electrostatic discharge voltage (Charged Device Model)	1250 V	500 V	These are at the component level ESD specifications and do not have any impact on the system level ESD, even though ESD values for CY15B256J-SXA are lower than FM24V02-G.
	Standby current (ISB), typical	80 μA	90 μA	Marginal increase in the typical value. The max current spec remains identical.
	Sleep current (IZZ), typical	4 μA	5 μA	
	Output LOW voltage (for VOL = 0.2 V, max)	IOL = 150 μA for VDD ≥ 2.0 V	Not specified	Improvement in the spec. CY15B256J-SXA follows the NXP standard I2C spec.
	Output LOW voltage (for VOL = 0.4 V, max)	IOL = 2 mA for VDD ≥ 2.7 V	IOL = 2 mA for VDD ≥ 2.0 V	
	Output LOW voltage (for VOL = 0.6 V, max)	Not specified	IOL = 6 mA for VDD ≥ 2.0 V	
	Data in hold (tHD:DAT), Max @ 3.4 MHz I2C	Not specified	70 ns	Improvement in the spec. CY15B256J-SXA follows the NXP standard I2C spec.
	Input rise time (tR), Min @ 3.4 MHz I2C	Not specified	10 ns	
	Input fall time (tF), Min @ 3.4 MHz I2C	Not specified	10 ns	
	Input fall time (tF), Min @ 1.0 MHz I2C	Not specified	20 * (VDD / 5.5 V)	
	ACK output valid time (tVD:ACK)	Not specified	Specified, meets NXP I2C spec	
	Output fall time from VIH min to VIL max	Not specified	Specified, meets NXP I2C spec	
	Power-up VDD (min) to first access (START condition)	250 μs	1000 μs	If the system boots up faster than 1000 μs, this difference needs to be adjusted to meet power up to first access time for CY15B256J-SXA. If the system boots up slower than 1000 μs, this difference doesn't trigger any change.



DATASHEET COMPARISON

Migrating from FM24V01-G to CY15B128J-SXA	Parameter	FM24V01 (Old Part)	CY15B128J (New Part)	Comments
	Device ID	004100h	004121h	If the device ID is used then the system firmware/software will require update.
	Surface mount lead soldering temperature	260 °C for 10 seconds	260 °C for 3 seconds	The surface mount lead soldering temperature of 260 °C for 3 seconds allows up to three reflow cycles. Therefore, the soldering spec of both devices are the same, but stated differently. Refer to the following website for more details: http://www.cypress.com/?docID=29889
	Electrostatic discharge voltage (Human Body Model)	3500 V	2000 V	No impact at the system level.
	Electrostatic discharge voltage (Charged Device Model)	1250 V	500 V	These are at the component level ESD specifications and do not have any impact on the system level ESD, even though ESD values for CY15B128J-SXA are lower than FM24V01-G.
	Standby current (ISB), typical	80 µA	90 µA	Marginal increase in the typical value. The max current spec remains identical.
	Sleep current (IZZ), typical	4 µA	5 µA	
	Output LOW voltage (for VOL = 0.2 V, max)	IOL = 150 µA for VDD ≥ 2.0 V	Not specified	
	Output LOW voltage (for VOL = 0.4 V, max)	IOL = 2 mA for VDD ≥ 2.7 V	IOL = 2 mA for VDD ≥ 2.0 V	
	Output LOW voltage (for VOL = 0.6 V, max)	Not specified	IOL = 6 mA for VDD ≥ 2.0 V	Improvement in the spec. CY15B128J-SXA follows the NXP standard I2C spec.
	Thermal resistance (θJA, junction to ambient)	145 °C/W	146 °C/W	The higher thermal resistance of CY15B128J-SXA will cause net increase in the maximum junction temp by ~3x10-4 °C, which is negligible.
	Data in hold (tHD-DAT), Max @ 3.4 MHz I2C	Not specified	70 ns	Improvement in the spec. CY15B128J-SXA follows the NXP standard I2C spec.
	Input rise time (tR), Min @ 3.4 MHz I2C	Not specified	10 ns	
	Input fall time (tF), Min @ 3.4 MHz I2C	Not specified	10 ns	
	Input fall time (tF), Min @ 1.0 MHz I2C	Not specified	20 * (VDD / 5.5 V)	
	ACK output valid time (tVD-ACK)	Not specified	Specified, meets NXP I2C spec	
	Output fall time from VIH min to VIL max	Not specified	Specified, meets NXP I2C spec	
	Power-up VDD (min) to first access (START condition)	250 µs	1000 µs	If the system boots up faster than 1000 µs, this difference needs to be adjusted to meet power up to first access time for CY15B128J-SXA. If the system boots up slower than 1000 µs, this difference doesn't trigger any change.

Migrating from FM25V01-G to CY15B128Q-SXA	Parameter	FM25V01 (Old Part)	CY15B128Q (New Part)	Comments
	Reserved opcode	No specified	11000011b 11000010b 01011010b 01011011b	No change. These reserved opcodes do exist in the FM25V01-G parts but were not shown in the datasheet.
	Device ID	7F7F7F7F7FC22100h	7F7F7F7F7FC22188h	A system software update is required to update the device ID when migrating to the FM25V01A-G.
	Electrostatic discharge voltage (Human Body Model)	1000 V	2000 V	Improvement in the CY15B128Q-SXA part but no impact at the system level.
	Electrostatic discharge voltage (Charged Device Model)	1250 V	500 V	These are at the component level ESD specifications and do not have any impact on the system level ESD.
	Electrostatic discharge voltage (Machine Model)	200	Not specified	JEDEC has discontinued use of the Machine Model (MM) because the MM is redundant to HBM at the device level. Cypress follows JEDEC standard ESD qualification, therefore the Machine Model ESD specification is not provided.
	Input resistance (/HOLD pin), for VIN = VIH (min)	40 kΩ	30 kΩ	The CY15B128Q-SXA internal pull-up resistor on the /HOLD pin is ~20% stronger. This provides better noise immunity. However, this reduction in the resistor value increases the leakage current by ~20%.
	Input resistance (/HOLD pin), for VIN = VIL (max)	1000 kΩ	800 kΩ	
	Thermal resistance (θJA, junction to ambient)	145 °C/W	146 °C/W	The higher thermal resistance of the CY15B128Q-SXA part will cause net increase in the maximum junction temp by ~3x10-4 °C, which is negligible.
	Clock HIGH time (tCH) for SCK = 25 MHz	20 ns	18 ns	This is an improvement in the CY15B128Q-SXA part. This allows the master SPI clock (SCK) duty cycle variations in the range of 45% to 55%.
	Clock LOW time (tCL) for SCK = 25 MHz	20 ns	18 ns	
	Output data valid time (tODV)	18 ns	16 ns	This is an improvement in the CY15B128Q-SXA part. Data at the output will be available 2 ns earlier hence using CY15B128Q-SXA provides more setup time for the host controller data input pin.
	Power-up VDD (min) to first access (/CS LOW)	250 µs	1000 µs	If the system boots up faster than 1000 µs, this difference needs to be adjusted to meet power up to first access time for CY15B128Q-SXA. If the system boots up slower than 1000 µs, this difference doesn't trigger any change.