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PRODUCT INFORMATION NOTIFICATION

PIN: PIN135258 **Date:** December 15, 2013

Subject: Qualification of JCET as an additional Test and Finish Location for Cypress Products

To: PCN ADMINISTRATOR
CYPRESS PCN ADMIN
pcn_adm@cypress.com

Change Type: Major

Description of Change:
Cypress announces the planned qualification of package-level Test and Finish manufacturing operations at Jiangsu Changjiang Electronics Technology Co., Ltd (JCET) in China for Cypress products that are currently being assembled at JCET and tested at King Yuan Electronics Co., Ltd., (KYEC) Taiwan and ChipMOS Technologies Inc., Hsinchu, Taiwan. There will not be any changes on the tester platforms, test program coverage and methodologies.

Current Flow	Assy (JCET-China)	==>	Test (Chipmos-Taiwan) Test (KYEC-Taiwan)	==>	Finish (Chipmos-Taiwan) Finish (KYEC-Taiwan)
Turnkey Flow	Assy (JCET-China)	==>	Test (JCET-China)	==>	Finish (JCET-China)

JCET is the largest provider of independent semiconductor manufacturing services in assembly and test in China. Their assembly facility in Changjiang, China is already a qualified assembly site for Cypress products. This qualification will enable these products to be assembled, tested and finish processed in one subcontractor facility. This qualification will allow Cypress to leverage JCET's manufacturing expertise and quality focus. This in turn also provides the means for Cypress to continue to meet its customers' IC testing needs as well as delivery commitments in dynamic, changing market conditions. JCET is certified on several international quality standards: ISO / TS16949: 2009, ANSI/ESD S20.20:2007, IECQ QC 080000:2005, ISO14001 and OHSAS18001.

Benefit of Change:
This change will provide a turnkey solution for these products that are being manufactured in Cypress' subcontractors. This will provide a faster delivery of products to Cypress' customers.

Affected Part Numbers: 655
Affected Parts: Please see the attached file for the list of parts affected by this notice.

Customer Part Numbers Affected
Affected Parts: N/A

Qualification Status:
The qualification report for 44TSOPII package that was processed on Advantest test Platform can be found as an attachment to this notification or by visiting www.cypress.com, typing the QTP number in the search window, and clicking on the magnifying glass icon. The qualification report for other package types and tester platforms will be available in January 2014 or February 2014.

Please refer to table below for the complete qualification schedules. Note that the schedules are estimated dates based on current projections, and are subject to change.

Tester Platform	QTP Number	Expected Date of Completion
ADVANTEST	133704	December 2013 to February 2014
VERSA 2104	133806	February 2014
VERSA 3308	133806	February 2014
NEXTEST	133805	January 2014
FINISH PROCESS	133803	December 2013 to January 2014

Approximate PIN Implementation Date:
Implementation is expected to start in December 2013 and be complete by March 2014.

Anticipated Impact:
Products that will be tested at JCET China will be completely compatible with existing product from a functional, parametric, and quality performance perspective.

Cypress also recommends that customers take this opportunity to review these changes against current application notes, system design considerations and customer environment conditions to assess impact (if any) to their application.

Method of Identification:
Cypress maintains traceability of product to wafer level, including wafer fabrication location, through the lot number marked on the package.

Response Required:
This is an information announcement only. No response is required

For additional information regarding this change, contact your local sales representative or contact the PCN Administrator at pcn_adm@cypress.com.

Sincerely,
Cypress PCN Administration