Appendix B
i.MX 6Solo/6DualLite Revision History

B.1 Substantive changes from revision 1 to revision 2

Substantive changes from revision 1 to revision 2 are as follows:

B.1.1 Reference Manual Revision History

No substantive changes

B.1.2 Architecture Overview Revision History

No substantive changes

B.1.3 Memory Maps Revision History

No substantive changes

B.1.4 Interrupts Revision History

No substantive changes

B.1.5 External Signals Revision History

No substantive changes

B.1.6 Fusemap Revision History

Reference	Description
Fusemap Description Table	Updated column two of row "0x450[15:8] (BOOT_CFG2)" in the SD/eSD Boot Fusemap table from reserved to include a description.
Fusemap Description Table	Added two additional rows.
Boot Fusemap	Update to 0x450[31:24] (BOOT_CFG4) column 7.
Fusemap Description Table	Added a row for temperature grade.
Boot Fusemap	Changed all instances of MMC_DDL_DLY address to 0x470[31:24].

B.1.7 External Memory Controllers Revision History

No substantive changes

B.1.8 System Debug Revision History

No substantive changes

B.1.9 System Boot Revision History

Reference	Description
NAND eFUSE Configuration	Updated BOOT_CFG1[1:0] fuse definition to read "Row Address Cycles" vs. "Adress Cycles".
HAB API Vector Table Addresses	Added vector address table.

B.1.10 Multimedia Revision History

No substantive changes

B.1.11 Power Management Revision History

No substantive changes

B.1.12 System Security Revision History

No substantive changes

B.1.13 ARM A9 Revision History

No substantive changes

B.1.14 AIPSTZ Revision History

Reference	Description
-	Updated memory map.

B.1.15 APBH Revision History

No substantive changes

B.1.16 ASRC Revision History

No substantive changes

B.1.17 AUDMUX Revision History

Reference	Description
Normal Mode	Updated text to read, "PTCR2's RFSEL[3:0] and RCSEL[3:0] must be set to 011b while PTCR4's RFSDIR and RCLKDIR set to 0." Previously read, "...RCKDIR set to 1".

B.1.18 CCM Revision History

Reference	Description
Clock Root Generator	Clock root generator figures updated.
CCM Memory Map/Register Definition	CCM_CLPCR register updated.
External Signals	External Signal table updated.

Table continues on the next page...

Reference	Description
CCM Clock Tree	Clock tree updated
Entering WAIT mode	Removed some internal information re: gating.
System Clocks	Updated max freq of IPU1_HSP_CLK_ROOT and IPU2_HSP_CLK_ROOT to 264 from 266.
CCM Memory Map/Register Definition	Minor updates to clock names. PLL3 inputs to clock root muxes updated to pll3_sw_clk.
Clock Switching Multiplexers	New topic added
-	References to pll2_sw_clk and related programming removed
System Clocks	System clocks, gating and override table updated
Clock Root Generator	Branch figures updated
CCM Clock Tree	Clock tree updated

B.1.19 CSI2IPU Revision History

No substantive changes

B.1.20 DCIC Revision History

No substantive changes

B.1.21 ECSPI Revision History

No substantive changes

B.1.22 EIM Revision History

Reference	Description
Burst (Synchronous Mode) Write Memory Access Timing - BCD=1	Added new topic to timing diagram section.

B.1.23 ENET Revision History

No substantive changes

B.1.24 EPDC Revision History

No substantive changes

B.1.25 EPIT Revision History

No substantive changes

B.1.26 ESAI Revision History

Reference	Description
ESAI Memory Map/Register Definition	Updated THCKP bit field description in the ESAI_TCCR register.

B.1.27 FLEXCAN3 Revision History

No substantive changes

B.1.28 GPC Revision History

No substantive changes

B.1.29 GPIO Revision History

Reference	Description
GPIO pad structure	GPIO pad structure topics added.

B.1.30 GPMI Revision History

No substantive changes

B.1.31 GPT Revision History

No substantive changes

B.1.32 GPU2D Revision History

No substantive changes

B.1.33 GPU3D Revision History

No substantive changes

B.1.34 HDMI Revision History

Reference	Description
HDMI Memory Map/Register Definition	Updated HDMI_IH_MUTE register.
HDMI Memory Map/Register Definition	HDMI_FC_INVIDCONF register definition added

B.1.35 HDMI PHY Revision History

No substantive changes

B.1.36 I2C Revision History

No substantive changes

B.1.37 IOMUXC Revision History

Reference	Description
-	DRAM_RESET setting updated. Pull/Keep functionality disabled on DRAM pads with exception of DRAM_DATAn and DRAM_SDQSn.
-	Cross-reference links added to pad groups.
-	Pad control register DSE fields for GPIO pad types (EIM, DI, ENET, NAND, CSI, SD, KEY, DISP, GPIO) updated.
-	SPEED field values updated for GPIO Pad types. Note added to related SPEED and SRE fields.

B.1.38 IPU Revision History

No substantive changes

B.1.39 KPP Revision History

No substantive changes

B.1.40 LDB Revision History

No substantive changes

B.1.41 MIPI CSI Revision History

No substantive changes

B.1.42 MIPI DSI Revision History

No substantive changes

B.1.43 MIPI HSI Revision History

No substantive changes

B.1.44 MLB150 Revision History

No substantive changes

B.1.45 MMDC Revision History

Reference	Description
MMDC Profiling	Added information regarding busy cycles in MADPSR1 (Busy cycles count) bullet.
MMDC Memory Map/Register Definition	Updated MMDC_MDASP bitfield description.

Table continues on the next page...

Reference	Description
MMDC Memory Map/Register Definition	Added note to WALAT bitfield description.
External Signals	External signal direction updated.

B.1.46 NIC Revision History

No substantive changes

B.1.47 OCOTP Revision History

No substantive changes

B.1.48 OCRAM Revision History

No substantive changes

B.1.49 PCIe Ctrl Revision History

No substantive changes

B.1.50 PCIe PHY Revision History

No substantive changes

B.1.51 PMU Revision History

Reference	Description
PMU	Updates to PMU_REG_Core.
Digital LDO Regulators	New note at end of section.

B.1.52 PWM Revision History

No substantive changes

B.1.53 PXP Revision History

No substantive changes

B.1.54 ROMCP Revision History

Reference	Description
ROMCP Memory Map/Register Definition	ROMCP Data Register instance value order updated.

B.1.55 SDMA Revision History

Reference	Description
Low Power Modes and User Control	Removed CRC column from power modes table.

B.1.56 SJC Revision History

No substantive changes

B.1.57 SNVS Revision History

No substantive changes

B.1.58 SPBA Revision History

No substantive changes

B.1.59 SPDIF Revision History

No substantive changes

B.1.60 SRC Revision History

No substantive changes

B.1.61 SSI Revision History

No substantive changes

B.1.62 TEMPMON Revision History

No substantive changes

B.1.63 TZASC Revision History

No substantive changes

B.1.64 UART Revision History

Reference	Description
External Signals	New figure for external signal path in DCE and DTE mode.

B.1.65 USB Revision History

No substantive changes

B.1.66 USB PHY Revision History

Reference	Description
USB_ANALOG	Update register bit description of USB_ANALOG_DIGPROG.

B.1.67 USDHC Revision History

No substantive changes

B.1.68 VDOA Revision History

No substantive changes

B.1.69 VPU Revision History

Reference	Description
Clocks	Update to the cclk row.

B.1.70 WDOG Revision History

No substantive changes

B.1.71 XTALOSC Revision History

Reference	Description
Overview	Update to block overview list.
Oscillator Configuration (32 kHz)	Updates to second paragraph.

B.1.72 SDMA Scripts Revision History

No substantive changes

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