0.13um FSL-KLM-FM PBGA Cu Wire Conversion (PCN 16799)

1. Objective

This report describes the Freescale Austin Technology Manufacturing Center (ATMC) fab site for 0.13um PBGA devices electrical distribution data on 20um PdCu wire versus baseline on 23um Au wire.

Current Wire:
MPC5200= 25um Au wire, MCF547X and MCF548X= 20um Au wire, MPC5200B= 23um Au wire

Proposed New Wire:
20um PdCu wire

2. General Information

Product Family: MPC5200, MCF547X, MCF548X, MPC5200B
Fab site: ATMC
Mask set: L25R, L14S, M62C
Package(s): 272 PBGA, 388 PBGA, 272 PBGAPGE
Assembly Site: Freescale Kuala Lumpur, Malaysia

3. Method

Two data sets taken from selected key product, 30 units in each set at T0 analysis:

1. 30 units from 20umPd Cu wire diameter qual lot from ATMC site
2. 30 units from 23um Au wire diameter control lot from ATMC fab site

Both qualification and control lots are tested to standard production final test flow. Electrical distribution data generated from the selected key parametric tests with Freescale standard criteria CPK > 1.67 and shift ≤ 15%, justification will be provided if otherwise.

4. Data and Summary:

4.1. Electrical Distribution Table:

Selected Evaluation Vehicle: MPC5554 (416PBGA) M68C
The ED data from Selected Evaluation Vehicle will be representing the parts stated in section 2 General Information

				Au Wire			Cu Wire			Shift within +/-1 sigma or less than 15% to spec LSL	Shift within +/-1 sigma or less than 15% to spec USL	Comment / Justification
				Temp	-40	C	Temp	-40	C			
Parameter Name, as in Datasheet	**Units**	**Lower Spec Limit** (NA if no spec)	**Upper Spec Limit** (NA if no spec)	**Avg**	**Std**	**Cpk**	**Avg**	**Std**	**Cpk**			
I/O input leakage vddeh high current pads etpu_a30	uA	-2.5	2.5	-0.0024	0.0062	134.52	-0.0129	0.0028	298.94	0.42%	0.42%	PASS
I/O input leakage vddeh high current pads etpu_a28	uA	-2.5	2.5	-0.0077	0.0050	165.67	-0.0078	0.0021	389.24	0.01%	0.01%	PASS
I/O input leakage vddeh low current pads etpu_a30	uA	-2.5	2.5	0.0016	0.0041	203.17	0.0013	0.0021	404.32	0.01%	0.01%	PASS
I/O input leakage vddeh low current pads etpu_a28	uA	-2.5	2.5	-0.0031	0.0031	272.86	0.0026	0.0027	311.26	0.23%	0.23%	PASS
I/O input leakage vddeh low current pads an13_sdo	uA	-2.5	2.5	-0.0016	0.0040	209.91	-0.0012	0.0029	289.66	0.02%	0.02%	PASS
I/O input leakage vddeh low current pads an15_fck	uA	-2.5	2.5	-0.0057	0.0022	371.26	0.0029	0.0021	388.97	0.34%	0.34%	PASS
I/O input leakage vdde high current pads addr17	uA	-2.5	2.5	-0.0049	0.0032	262.80	-0.0126	0.0025	330.65	0.31%	0.31%	PASS
I/O input leakage vdde high current pads addr19	uA	-2.5	2.5	0.0073	0.0039	214.15	-0.0055	0.0023	359.30	0.51%	0.51%	PASS
I/O input leakage vdde low current pads addr17	uA	-2.5	2.5	-0.0021	0.0036	231.96	-0.0031	0.0024	349.23	0.04%	0.04%	PASS
I/O input leakage vdde low current pads addr19	uA	-2.5	2.5	0.0066	0.0049	168.74	-0.0040	0.0023	359.52	0.42%	0.42%	PASS
I/O input leakage vdda low current pads an34	uA	-0.2	0.2	-0.0004	0.0003	154.03	0.0000	0.0003	167.03	0.23%	0.23%	PASS
I/O input leakage vdda low current pads an32	uA	-0.2	0.2	-0.0002	0.0003	145.61	-0.0007	0.0002	230.03	0.31%	0.30%	PASS
I/O input leakage vdda high current pads an34	uA	-0.2	0.2	-0.0004	0.0003	170.60	0.0013	0.0002	232.36	1.12%	1.11%	PASS
I/O input leakage vdda high current pads an32	uA	-0.2	0.2	-0.0011	0.0003	192.73	-0.0017	0.0003	170.30	0.37%	0.36%	PASS
I/O input leakage vdda high current pads an35	uA	-0.2	0.2	-0.0006	0.0002	206.44	-0.0015	0.0003	187.03	0.56%	0.56%	PASS
I/O input leakage vdda high current pads an33	uA	-0.2	0.2	-0.0005	0.0003	165.03	0.0001	0.0002	254.26	0.41%	0.40%	PASS
I/O weak pullup vdde current cs_b0	uA	-170	-20	-135.3699	2.6142	4.42	-137.3471	1.6403	6.64	5.71%	1.71%	PASS
I/O weak pullup vdde current cs_b1	uA	-170	-20	-135.6093	1.8787	6.10	-137.4545	1.9324	5.61	5.37%	1.60%	PASS
I/O weak pullup vdde current cs_b2	uA	-170	-20	-135.2591	2.1505	5.39	-137.1261	1.7586	6.23	5.37%	1.62%	PASS
I/O weak pulldown vdde current cs_b0	uA	20	170	95.7533	3.2114	7.71	99.4852	3.0764	7.64	4.93%	5.03%	PASS
I/O weak pulldown vdde current cs_b1	uA	20	170	96.2780	2.6326	9.33	98.4250	3.3067	7.22	2.81%	2.91%	PASS
I/O weak pulldown vdde current cs_b2	uA	20	170	96.5628	3.2369	7.56	98.0009	2.5148	9.54	1.88%	1.96%	PASS

				Au Wire			Cu Wire			Shift within +/-1 sigma or less than 15% to spec LSL	Shift within +/-1 sigma or less than 15% to spec USL	Comment / Justification
				Temp	-40	C	Temp	-40	C			
Parameter Name, as in Datasheet	**Units**	**Lower Spec Limit** (NA if no spec)	**Upper Spec Limit** (NA if no spec)	**Avg**	**Std**	**Cpk**	**Avg**	**Std**	**Cpk**			
I/O weak pullup vddeh current pllcfg0	uA	-170	-20	-117.4049	1.2051	14.55	-118.9035	0.9423	18.07	2.85%	1.54%	PASS
I/O weak pullup vddeh current pllcfg1	uA	-170	-20	-117.6931	1.2184	14.31	-119.4286	1.0111	16.67	3.32%	1.78%	PASS
I/O weak pullup vddeh current rstcfg_b	uA	-170	-20	-122.7166	1.4323	11.00	-124.2449	0.9841	15.50	3.23%	1.49%	PASS
I/O weak pulldown vddeh current pllcfg0	uA	20	170	69.9430	2.1928	7.59	70.6571	2.7308	6.18	1.43%	0.71%	PASS
I/O weak pulldown vddeh current pllcfg1	uA	20	170	70.2039	2.3120	7.24	70.5686	2.6317	6.41	0.73%	0.37%	PASS
I/O weak pulldown vddeh current rstcfg_b	uA	20	170	69.4987	2.0778	7.94	69.6991	2.4515	6.76	0.40%	0.20%	PASS
Current can be sourced by VRCCTL at Tj	mA	-25.0	-6.8	-12.8602	0.2092	9.66	-13.4220	0.1286	17.16	4.63%	9.27%	PASS
PLL maximum clamp	Mhz	135	300	188.1869	4.6750	3.79	194.2980	5.0995	3.88	11.49%	5.47%	PASS
PLL minimum clamp	Mhz	15	48	24.3401	0.9705	3.21	25.0748	0.9791	3.43	7.87%	3.11%	PASS
PLL lock time	uS	104.9	750.0	165.6167	4.3511	4.65	166.2600	5.7913	3.53	1.06%	0.11%	PASS
PLL cloop d1_mfd0	count	30.4	45.6	37.4667	1.1666	2.02	37.3000	0.6513	3.53	2.36%	2.05%	PASS
PLL cloop d2_mfd1	count	61.6	92.4	76.4667	1.1059	4.48	76.8667	1.1366	4.48	2.69%	2.51%	PASS
Run Idd vdde	mA	NA	70	30.1282	0.1573	84.47	30.7361	0.0717	182.42	NA	1.52%	PASS
Run Idd vddeh	mA	NA	140	96.7660	0.4285	33.63	96.6760	1.0755	13.43	NA	0.21%	PASS
Run Idd vdd33	mA	NA	5	0.7897	0.0031	458.78	0.7826	0.0036	390.40	NA	0.17%	PASS
Run Idd vddsyn	mA	NA	18	10.6182	0.1859	13.23	10.5656	0.1294	19.15	NA	0.71%	PASS
Run Idd	mA	NA	0.05	0.000012	0.000014	1205.72	0.0000	0.0000	2006.26	NA	0.06%	PASS
Run Idd vdd	mA	NA	700	526.3720	5.5505	10.43	528.0958	3.3514	17.10	NA	0.99%	PASS
Required gain at Tj	-	20	65	45.0331	0.7628	8.73	43.2849	0.5889	12.29	6.98%	8.76%	PASS
Stop Idd low range vdd	mA	NA	10	2.6416	0.1549	15.83	2.5644	0.1366	18.14	NA	1.05%	PASS
Program Erase cycle evenpage	cycle	NA	99999	4.0796	0.5821	57259.91	4.4510	0.4019	82926.44	NA	0.00%	PASS
Program Erase cycle oddpage	cycle	NA	99999	4.9914	0.5864	56836.70	5.3621	0.4038	82543.71	NA	0.00%	PASS
EQADC HV INL: 12 MHz ADC clock adc0INL_P -1	Count	-4	4	0.8572	0.1597	6.56	0.8407	0.1672	6.30	0.34%	0.53%	PASS
EQADC HV INL: 12 MHz ADC clock adc0INL_N -1	Count	-4	4	-0.7981	0.1658	6.44	-0.8179	0.1945	5.45	0.62%	0.41%	PASS
EQADC HV DNL: 12 MHz ADC clock adc0DNL_P -1	Count	-3	3	0.7403	0.0791	9.52	0.7429	0.0665	11.32	0.07%	0.12%	PASS
EQADC HV DNL: 12 MHz ADC clock adc0DNL_N -1	Count	-3	3	-0.7078	0.0406	18.81	-0.7139	0.0750	10.17	0.27%	0.16%	PASS
EQADC HV INL: 12 MHz ADC clock adc1INL_P -1	Count	-4	4	0.9077	0.1732	5.95	0.8663	0.2140	4.88	0.84%	1.34%	PASS
EQADC HV INL: 12 MHz ADC clock adc1INL_N -1	Count	-4	4	-0.7502	0.1723	6.29	-0.7909	0.1787	5.98	1.25%	0.86%	PASS
EQADC HV DNL: 12 MHz ADC clock adc1DNL_P -1	Count	-3	3	0.7428	0.0630	11.95	0.7417	0.0740	10.17	0.03%	0.05%	PASS
EQADC HV DNL: 12 MHz ADC clock adc1DNL_N -1	Count	-3	3	-0.6684	0.0661	11.75	-0.6977	0.0729	10.52	1.25%	0.80%	PASS
EQADC HV INL: 12 MHz ADC clock adc0INL_N -1	Count	-6	6	-0.8245	0.1229	14.04	-0.7157	0.1404	12.54	2.10%	1.59%	PASS
EQADC HV DNL: 12 MHz ADC clock adc0DNL_P -1	Count	-3	3	0.6968	0.0847	9.07	0.5965	0.0747	10.73	2.71%	4.36%	PASS
EQADC HV DNL: 12 MHz ADC clock adc0DNL_N -1	Count	-3	3	-0.5996	0.0441	18.13	-0.5598	0.0564	14.43	1.66%	1.11%	PASS
EQADC HV INL: 12 MHz ADC clock adc1INL_P -1	Count	-6	6	0.8073	0.1451	11.93	0.7253	0.1145	15.36	1.20%	1.58%	PASS
EQADC HV INL: 12 MHz ADC clock adc1INL_N -1	Count	-6	6	-0.7079	0.1294	13.63	-0.7112	0.1187	14.85	0.06%	0.05%	PASS
EQADC HV DNL: 12 MHz ADC clock adc1DNL_P -1	Count	-3	3	0.5583	0.0688	11.84	0.5494	0.0570	14.34	0.25%	0.36%	PASS
EQADC HV DNL: 12 MHz ADC clock adc1DNL_N -1	Count	-3	3	-0.5473	0.0611	13.38	-0.5569	0.0560	14.55	0.39%	0.27%	PASS
EQADC Disruptive input injection current	mA	0	20	7.7525	0.4820	5.36	7.7000	0.3889	6.60	0.68%	0.43%	PASS
EQADC Disruptive high input injection current	mA	0	1	0.2337	0.0097	8.04	0.2316	0.0093	8.27	0.90%	0.27%	PASS
EQADC Disruptive low input injection current	mA	-1	0	-0.1159	0.0028	13.75	-0.1186	0.0029	13.52	0.30%	2.29%	PASS

Parameter Name, as in Datasheet	Units	Lower Spec Limit (NA if no spec)	Upper Spec Limit (NA if no spec)	Au Wire Temp 145 C Avg	Au Wire Temp 145 C Std	Au Wire Temp 145 C Cpk	Cu Wire Temp 145 C Avg	Cu Wire Temp 145 C Std	Cu Wire Temp 145 C Cpk	Shift within +/-1 sigma or less than 15% to spec LSL	Shift within +/-1 sigma or less than 15% to spec USL	Comment / Justification
I/O input leakage vddeh high current pads etpu_a30	uA	-2.5	2.5	0.2022	0.0531	14.43	0.3213	0.0508	14.29	4.41%	5.19%	PASS
I/O input leakage vddeh high current pads etpu_a28	uA	-2.5	2.5	0.2032	0.0525	14.57	0.3141	0.0487	14.95	4.10%	4.83%	PASS
I/O input leakage vddeh low current pads etpu_a30	uA	-2.5	2.5	-0.0171	0.0046	178.32	-0.0245	0.0044	186.87	0.30%	0.30%	PASS
I/O input leakage vddeh low current pads etpu_a28	uA	-2.5	2.5	-0.0161	0.0043	193.21	-0.0214	0.0041	199.29	0.21%	0.21%	PASS
I/O input leakage vddeh low current pads an13_sdo	uA	-2.5	2.5	-0.0189	0.0037	220.98	-0.0280	0.0049	167.58	0.37%	0.36%	PASS
I/O input leakage vddeh low current pads an15_fck	uA	-2.5	2.5	-0.0152	0.0037	222.04	-0.0309	0.0047	175.33	0.63%	0.62%	PASS
I/O input leakage vdde high current pads addr17	uA	-2.5	2.5	0.0782	0.0415	19.47	0.1311	0.0277	28.52	2.05%	2.18%	PASS
I/O input leakage vdde high current pads addr19	uA	-2.5	2.5	0.0897	0.0293	27.46	0.1432	0.0219	35.95	2.07%	2.22%	PASS
I/O input leakage vdde low current pads addr17	uA	-2.5	2.5	-0.0696	0.0107	75.48	-0.0900	0.0064	125.31	0.84%	0.80%	PASS
I/O input leakage vdde low current pads addr19	uA	-2.5	2.5	-0.0702	0.0106	76.49	-0.0849	0.0070	115.69	0.60%	0.57%	PASS
I/O input leakage vdda low current pads an34	uA	-0.2	0.2	-0.0006	0.0003	185.21	-0.0011	0.0003	186.71	0.34%	0.34%	PASS
I/O input leakage vdda low current pads an32	uA	-0.2	0.2	-0.0015	0.0003	150.08	-0.0010	0.0002	242.57	0.35%	0.34%	PASS
I/O input leakage vdda high current pads an34	uA	-0.2	0.2	0.0162	0.0034	13.31	0.0233	0.0033	12.90	4.29%	5.32%	PASS
I/O input leakage vdda high current pads an32	uA	-0.2	0.2	0.0140	0.0035	12.94	0.0227	0.0033	12.76	5.34%	6.44%	PASS
I/O input leakage vdda high current pads an35	uA	-0.2	0.2	0.0140	0.0035	13.03	0.0231	0.0033	12.74	5.55%	6.69%	PASS
I/O input leakage vdda high current pads an33	uA	-0.2	0.2	0.0153	0.0034	13.16	0.0231	0.0032	13.07	4.71%	5.77%	PASS
I/O weak pullup vdde current cs_b0	uA	-170	-20	-107.4475	1.3710	15.21	-106.3744	1.7096	12.41	1.72%	1.23%	PASS
I/O weak pullup vdde current cs_b1	uA	-170	-20	-107.6673	1.3816	15.04	-106.7778	1.6066	13.12	1.43%	1.01%	PASS
I/O weak pullup vdde current cs_b2	uA	-170	-20	-107.4700	1.5353	13.58	-106.4965	1.6466	12.86	1.56%	1.11%	PASS
I/O weak pulldown vdde current cs_b0	uA	20	170	80.4010	2.6709	7.54	79.3616	2.4959	7.93	1.72%	1.16%	PASS
I/O weak pulldown vdde current cs_b1	uA	20	170	81.1881	2.8249	7.22	79.9783	2.5346	7.89	1.98%	1.36%	PASS
I/O weak pulldown vdde current cs_b2	uA	20	170	80.9345	2.2904	8.87	80.8651	2.3617	8.59	0.11%	0.08%	PASS
I/O weak pullup vddeh current pllcfg0	uA	-170	-20	-84.6634	0.8015	26.89	-83.3219	0.7033	30.01	1.57%	2.07%	PASS
I/O weak pullup vddeh current pllcfg1	uA	-170	-20	-84.9283	0.7935	27.27	-83.3972	0.7276	29.05	1.80%	2.36%	PASS
I/O weak pullup vddeh current rstcfg_b	uA	-170	-20	-88.0596	0.7839	28.94	-86.2111	0.7152	30.86	2.26%	2.72%	PASS
I/O weak pulldown vddeh current pllcfg0	uA	20	170	60.3210	1.4487	9.28	58.6037	1.8113	7.10	4.26%	1.57%	PASS
I/O weak pulldown vddeh current pllcfg1	uA	20	170	60.5472	1.3958	9.68	58.5440	1.8399	6.98	4.94%	1.83%	PASS
I/O weak pulldown vddeh current rstcfg_b	uA	20	170	59.7089	1.3234	10.00	58.5340	1.6515	7.78	2.96%	1.07%	PASS
Current can be sourced by VRCCTL at Tj	mA	-25.0	-6.8	-9.4923	0.1151	7.79	-9.0990	0.1686	4.54	2.54%	14.61%	PASS
PLL maximum clamp	Mhz	135	300	179.1111	2.4459	6.01	178.9646	2.8054	5.22	0.33%	0.12%	PASS
PLL minimum clamp	Mhz	15	48	27.5578	0.7140	5.86	28.0204	0.8527	5.09	3.68%	2.26%	PASS
PLL lock time	uS	104.9	750.0	164.5200	3.7357	5.32	167.4167	4.5978	4.53	4.86%	0.49%	PASS
PLL cloop d1_mfd0	count	22.8	53.2	38.0333	0.7649	6.61	38.6333	0.8087	6.00	3.94%	3.96%	PASS
PLL cloop d2_mfd1	count	46.2	107.8	76.8000	0.8469	12.04	77.5000	0.9377	10.77	2.29%	2.26%	PASS
Run Idd vdde	mA	NA	70	38.6568	0.3381	30.90	37.5866	0.1410	76.65	NA	3.41%	PASS
Run Idd vddeh	mA	NA	140	96.3179	0.4431	32.86	94.6231	0.6566	23.04	NA	3.88%	PASS
Run Idd vdd33	mA	NA	5	0.8642	0.0035	388.34	0.8630	0.0035	398.01	NA	0.03%	PASS
Run Idd vddsyn	mA	NA	18	11.5498	0.1719	12.51	11.4836	0.1487	14.61	NA	1.03%	PASS
Run Idd	mA	NA	0.1	0.0000	0.0000	1809.60	0.0000	0.0000	1090.76	NA	0.04%	PASS
Run Idd vdd	mA	NA	700	547.9494	5.3013	9.56	525.7219	7.5791	7.66	NA	14.62%	PASS
Required gain at Tj	-	20	91	63.5071	0.9873	9.28	63.5653	0.8365	10.93	0.13%	0.21%	PASS
Stop Idd low range vdd	mA	NA	210	12.1040	1.5387	42.87	19.5989	2.2921	27.69	NA	3.79%	PASS
Program Erase cycle evenpage	cycle	NA	99999	17.8668	0.4455	74800.30	16.9157	0.5138	64858.36	NA	0.00%	PASS
Program Erase cycle oddpage	cycle	NA	99999	18.7410	0.4535	73485.27	17.7793	0.5213	63927.18	NA	0.00%	PASS
EQADC Disruptive input injection current	mA	0	20	8.1552	0.3223	8.43	8.1478	0.3156	8.60	0.09%	0.06%	PASS
EQADC Disruptive high input injection current	mA	0	1	0.2112	0.0077	9.12	0.2079	0.0071	9.79	1.60%	0.43%	PASS
EQADC Disruptive low input injection current	mA	-1	0	-0.0824	0.0019	14.69	-0.0794	0.0016	16.13	0.33%	3.64%	PASS

“Shift analysis” refers to analysis of shift of the distribution mean towards the nearest specification limit:
“% Shift (USL) = {Mean(new)-Mean(old)} / {Upper Spec Limit-Mean(old)}
% Shift (LSL) = {Mean(new)-Mean(old)} / {Mean(old)-Lower Spec Limit}

4.2. Summary:

From the above data, it was verified that the requirements and acceptance criteria was achieved.

5. Document History:

Rev	Date	Originator
O	28th May 2015	YANG Lei-B46636