Freescale PCN 16360

862B Electrical Characterization (DC Parameters)

				Hot Temperature			
				Qual Lot #1	Qual Lot #2	Qual Lot #3	Control
Test	Pin	Description	Unit	Cpk	Cpk	Cpk	Cpk
DC Characterization VIL VIH VOL VOH	vilp	input low voltage	V	> 1.67	> 1.67	> 1.67	> 1.67
	vihp	input high voltage	V	> 1.67	> 1.67	> 1.67	> 1.67
	volp	output low voltage	V	> 1.67	> 1.67	> 1.67	> 1.67
	vohp	output high voltage	V	> 1.67	> 1.67	> 1.67	> 1.67

				Room Temperature			
				Qual Lot #1	Qual Lot #2	Qual Lot #3	Control
Test	Pin	Description	Unit	Cpk	Cpk	Cpk	Cpk
DC Characterization VIL VIH VOL VOH	vilp	input low voltage	V	> 1.67	> 1.67	> 1.67	> 1.67
	vihp	input high voltage	V	> 1.67	> 1.67	> 1.67	> 1.67
	volp	output low voltage	V	> 1.67	> 1.67	> 1.67	> 1.67
	vohp	output high voltage	V	> 1.67	> 1.67	> 1.67	See Note 1

				Cold Temperature			
				Qual Lot #1	Qual Lot #2	Qual Lot #3	Control
Test	Pin	Description	Unit	Cpk	Cpk	Cpk	Cpk
DC Characterization VIL VIH VOL VOH	vilp	input low voltage	V	> 1.67	> 1.67	> 1.67	> 1.67
	vihp	input high voltage	V	> 1.67	> 1.67	> 1.67	> 1.67
	volp	output low voltage	V	> 1.67	> 1.67	> 1.67	> 1.67
	vohp	output high voltage	V	> 1.67	> 1.67	> 1.67	See Note 1

Note 1: No variability across sample. Cpk not calculated.

Freescale PCN 16360

862B Electrical Characterization (AC Parameters) Cpk's < 1.67 are 100% covered by the test program				Hot Temperature				Room Temperature				Cold Temperature			
				Qual Lot #1	Qual Lot #2	Qual Lot #3	Control	Qual Lot #1	Qual Lot #2	Qual Lot #3	Control	Qual Lot #1	Qual Lot #2	Qual Lot #3	Control
Test	Spec	Description	Unit	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk
AC Characterization Using Serial Patterns @ 50MHz	sp8:	CLKOUT to A(0:31), BADDR(28:30)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp8a:	CLKOUT to TSIZ(0:1), REG, RSV,	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp8b:	CLKOUT to BR, BG, VFLS(0:1),	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp11a:	CLKOUT to TA,BI Assertion(when drv by Mem Ctrl	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp12a:	CLKOUT to TA,BI Negation(when drv by Mem Ctrl	ns	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1
	sp16a:	TEA, KR, RETRY, CR valid to CLKOUT (setup time)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp16b:	BB,BG,BR Valid to CLKOUT - Setup	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp18:	Date,DP Valid to CLKOUT Rise Edge - Setup	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp19:	CLKOUT Rise Edge to Data,DP Valid - Hold	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp25:	CLKOUT Rise Edge to OE, WE Asserted	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp32b:	CLKOUT Rise to BS Valid (Per BST2 in the UPM)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp52:	CLKOUT to ALE assert time	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp64:	DSCK High to DSDO Data Valid	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp31s:	Clock High To Data-Out Valid (CPU Write Data, cntl, dir.)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp73s:	L1RSYNC,L1TSYNC Valid To L1CLK Edge (Sync Setup)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp78s:	L1CLK Edge To L1ST(1-4) Valid	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp80s:	L1CLK Edge To L1TDX Valid	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp84s:	L1CLK Edge to L1CLKO Valid (DSC=1)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp103:	TXD1 active delay (from TCLK1 falling edge)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp131:	TXD1 active delay (from TCLK1 rising edge)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp133:	TENA active delay (from TCLK1 rising edge)	ns	>1.67	>1.67	See Note 1	See Note 1	See Note 1	>1.67	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1

Note 1: No variability across sample. Cpk not calculated.

Freescale PCN 16360

862B Electrical Characterization (AC Parameters) Cpk's < 1.67 are 100% covered by the test program				Hot Temperature				Room Temperature				Cold Temperature			
				Qual Lot #1	Qual Lot #2	Qual Lot #3	Control	Qual Lot #1	Qual Lot #2	Qual Lot #3	Control	Qual Lot #1	Qual Lot #2	Qual Lot #3	Control
Test	Spec	Description	Unit	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk
AC Characterization Using 1:1 50MHz Bus Patterns	sp8:	CLKOUT to A(0:31), BADDR(28:30)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp8a:	CLKOUT to TSIZ(0:1), REG, RSV,	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp8b:	CLKOUT to BR, BG, VFLS(0:1),	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp11a:	CLKOUT to TA, BI assertion (when	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp12:	CLKOUT to TS, BB negation (MAX =	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp12a:	CLKOUT to TA, BI negation (when	ns	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1
	sp16:	TA, BI valid to CLKOUT (setup time)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp17:	CLKOUT to TA, TEA, BI, BB, BG, BR	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp18:	D(0:31), DP(0:3) valid to CLKOUT	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp19:	CLKOUT rising edge to D(0:31),	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp22:	CLKOUT rising edge to CS asserted	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp25:	CLKOUT rising edge to OE, WE(0:3)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp28:	CLKOUT rising edge to WE(0:3)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp31:	CLKOUT falling edge to CS valid - as	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp31c:	CLKOUT rising edge to CS valid - as	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp32:	CLKOUT falling edge to BS valid- as	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp32b:	CLKOUT rising edge to BS valid - as	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	<1.67	>1.67	>1.67	>1.67
	sp32c:	CLKOUT rising edge to BS valid - as	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp33a:	CLKOUT rising edge to GPL Valid - as	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp52:	CLKOUT to ALE assert time	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
UTOPIA AC Electrical Specifications	usp1	UtpClk rise/fall time (Internal clock option)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	usp2	RxEnb and TxEnb active delay	ns	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1
	usp5	UTPB, SOC active delay (and PHREQ and PHSEL active	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
FEC Electrical Characteristics	m2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	m6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67

Note 1: No variability across sample. Cpk not calculated.

Freescale PCN 16360

860D4 Electrical Characterization (DC Parameters)

				Hot Temperature			
				Qual Lot #1	Qual Lot #2	Qual Lot #3	Control
Test	Pin	Description	Unit	Cpk	Cpk	Cpk	Cpk
DC Characterization VIL VIH VOL VOH	vilp	input low voltage	V	> 1.67	> 1.67	> 1.67	> 1.67
	vihp	input high voltage	V	> 1.67	> 1.67	See Note 1	> 1.67
	volp	output low voltage	V	> 1.67	> 1.67	> 1.67	> 1.67
	vohp	output high voltage	V	> 1.67	> 1.67	> 1.67	See Note 1

				Room Temperature			
				Qual Lot #1	Qual Lot #2	Qual Lot #3	Control
Test	Pin	Description	Unit	Cpk	Cpk	Cpk	Cpk
DC Characterization VIL VIH VOL VOH	vilp	input low voltage	V	> 1.67	> 1.67	> 1.67	> 1.67
	vihp	input high voltage	V	> 1.67	> 1.67	> 1.67	> 1.67
	volp	output low voltage	V	> 1.67	> 1.67	> 1.67	> 1.67
	vohp	output high voltage	V	> 1.67	See Note 1	See Note 1	See Note 1

				Cold Temperature			
				Qual Lot #1	Qual Lot #2	Qual Lot #3	Control
Test	Pin	Description	Unit	Cpk	Cpk	Cpk	Cpk
DC Characterization VIL VIH VOL VOH	vilp	input low voltage	V	> 1.67	> 1.67	> 1.67	> 1.67
	vihp	input high voltage	V	> 1.67	> 1.67	> 1.67	> 1.67
	volp	output low voltage	V	> 1.67	> 1.67	> 1.67	> 1.67
	vohp	output high voltage	V	> 1.67	> 1.67	> 1.67	> 1.67

Note 1: No variability across sample. Cpk not calculated.

Freescale PCN 16360

860D4 Electrical Characterization (AC Parameters)

				Hot Temperature				Room Temperature				Cold Temperature			
				Qual Lot #1	Qual Lot #2	Qual Lot #3	Control	Qual Lot #1	Qual Lot #2	Qual Lot #3	Control	Qual Lot #1	Qual Lot #2	Qual Lot #3	Control
Test	Spec	Description	Unit	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk
AC Characterization Using Serial Patterns @ 50MHz	sp8:	CLKOUT to A(0:31), BADDR(28:30)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp8a:	CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp8b:	CLKOUT to BR, BG, VFLS(0:1), VF(0:2),	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp11a:	CLKOUT to TA, BI assertion (when driven by	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp12a:	CLKOUT to TA, BI negation (when driven by	ns	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1
	sp16a:	TEA, KR, RETRY, CR valid to CLKOUT	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp16b:	BB, BG, BR, valid to CLKOUT (setup time)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp18:	D(0:31), DP(0:3) valid to CLKOUT rising	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp19:	CLKOUT rising edge to D(0:31), DP(0:3)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp25:	CLKOUT rising edge to OE, WE(0:3)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp32b:	CLKOUT rising edge to BS valid—as	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp52:	CLKOUT to ALE assert time	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp64:	DSCK High to DSDO Data Valid	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp31s:	Clock low to data-out valid	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp73s:	L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp78s:	L1CLK edge to L1ST(1–4) valid	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp80s:	L1CLK edge to L1TXD valid	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp84s:	L1CLK edge to L1CLKO valid	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp103:	TXD1 active delay (from TCLK1 falling edge)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp131:	TXD1 active delay (from TCLK1 rising edge)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp133:	TENA active delay (from TCLK1 rising edge)	ns	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1

Note 1: No variability across sample. Cpk not calculated.

Freescale PCN 16360

860D4 Electrical Characterization (AC Parameters)

				Hot Temperature				Room Temperature				Cold Temperature			
				Qual Lot #1	Qual Lot #2	Qual Lot #3	Control	Qual Lot #1	Qual Lot #2	Qual Lot #3	Control	Qual Lot #1	Qual Lot #2	Qual Lot #3	Control
Test	Spec	Description	Unit	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk	Cpk
AC Characterization Using 1:1 50MHz Bus Patterns	sp8:	CLKOUT to A(0:31), BADDR(28:30)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp8a:	CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp8b:	CLKOUT to BR, BG, VFLS(0:1),	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp11a:	CLKOUT to TA, BI assertion (when driven by	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp12:	CLKOUT to TS, BB negation	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp12a:	CLKOUT to TA, BI negation (when driven by	ns	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1
	sp16:	TA, BI valid to CLKOUT (setup time)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp17:	CLKOUT to TA, TEA, BI, BB, BG, BR valid	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp18:	D(0:31), DP(0:3) valid to CLKOUT rising	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp19:	CLKOUT rising edge to D(0:31), DP(0:3)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp22:	CLKOUT rising edge to CS asserted GPCM	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp25:	CLKOUT rising edge to OE, WE(0:3)	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp28:	CLKOUT rising edge to WE(0:3) negated	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp31:	CLKOUT falling edge to CS valid—as	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp31c:	CLKOUT rising edge to CS valid—as	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp32:	CLKOUT falling edge to BS valid—as	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp32b:	CLKOUT rising edge to BS valid—as	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp32c:	CLKOUT rising edge to BS valid—as	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp33a:	CLKOUT rising edge to GPL valid—as	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	sp52:	CLKOUT to ALE assert time	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
FEC Electrical Characteristics	m2	II_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	ns	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67	>1.67
	m6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	ns	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1

Note 1: No variability across sample. Cpk not calculated.