

Worked on: Michael Madden on: 2015-01-13

For integrated circuits or discrete semiconductors select below:

AEC-Q100

PCN number 16548

				Evaluation level A1/B/C		Remarks / Comments	
		Understanding of semiconductors experts		Examples to explain			
Assessment of impact on Supply Chain regarding following aspects		Remaining risks on Supply Chain?		X: Not included P: Partially included C: Completely included I: Not relevant			
- contractual agreements - technical interface of processability/manufacturability of customer - form, fit, function, quality performance, reliability							
Type of change		No	Yes				
Any change with impact on agreed upon contractual agreements		P	P	Not relevant for technical evaluation		**	
Any change with impact on technical interface or processability/manufacturability of customer		I	P	Be info Note for cases where customer should be aware of and which are not named in this document.		+ A, B, C: Depends on change.	
DRAFT/REWORK							
Change of draft/rework parameters/electrical specification (min, max / p. values) and/or AC/DC specification <sup>1)</sup>		P	P	Change of application note/art information (e.g. for new material or new test method) P: Partially included; Editorial changes		A + Not included: Editorial changes	
Correction of data sheet / errata		I	P	Data sheet		A Errata sheet as information note in case of additional changes Errata sheet which impacts product integrity requires a PCN.	
DESIGN							
Design change in rating <sup>2)</sup>		P	P	Any change in chip design / layout. Not included: design optimization		+ A, B, C: Depends on change. + Not included: Design optimization = modification to adapt to the specified process window. + e.g. crack avoidance or metal dip	
Tests, which should be considered for the appropriate process change.						+	
Tests, which should be considered for the appropriate process change after selection of condition table.						+	
Suppliers performed tests (mark with an 'X' for done or 'O' for generic)							
Reason for exception of tests: All ROM Change only - no difference in any trait/characteristic, etc that would warrant a stress test to evaluate. Qualification with no Stress Evaluation was specifically approved by FSL AIX MCR business unit Change Action Board. Gate Leakage - Freescale does not perform as part of qualification							

- No
I Information Note required.
P PCN required.

A mark "X" indicates that performance or that stress test should be considered for the appropriate process change.		
CONDITIONS	YES	NO
B Only for peripheral routing	X	
C If bond to leadfinger	X	
D Design rule change	X	
E Process only	X	
F MBS only	X	
G Only from non-100% burn-in parts	X	
H Hermetic only	X	
I Leadframe required	X	
K Passivation only	X	
M For devices requiring PTC	X	
N Passivation and gate oxide	X	
O Wire diameter decrease	X	
S Required for plastic SMD only	X	
A1 Only if device uses CAN LIN, FLEXRAY	X	
A6 Only EMI/EMC testing is affected	X	
>> Please mark 'YES' or 'NO' with a small 'x'		