



PRODUCT AND PROCESS CHANGE NOTIFICATION UPDATE

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ISSUE DATE: 11-Mar-2015
 NOTIFICATION: 16548A
 TITLE: I.MX 6DUALLITE AND I.MX 6SOLO SILICON REVISION UPDATES
 EFFECTIVE DATE: 05-Jul-2015

DEVICE(S)

MPN
MCIMX6S1AVM08AB
MCIMX6S1AVM08ABR
MCIMX6S1AVM08AC
MCIMX6S1AVM08ACR
MCIMX6S4AVM08AB
MCIMX6S4AVM08ABR
MCIMX6S4AVM08AC
MCIMX6S4AVM08ACR
MCIMX6S5DVM10AB
MCIMX6S5DVM10ABR
MCIMX6S5DVM10AC
MCIMX6S5DVM10ACR
MCIMX6S5EVM10AB
MCIMX6S5EVM10ABR
MCIMX6S5EVM10AC
MCIMX6S5EVM10ACR
MCIMX6S6AVM08AB
MCIMX6S6AVM08ABR
MCIMX6S6AVM08AC
MCIMX6S6AVM08ACR
MCIMX6S7CVM08AB
MCIMX6S7CVM08AC
MCIMX6S8DVM10AB
MCIMX6S8DVM10AC
MCIMX6U1AVM08AB
MCIMX6U1AVM08ABR
MCIMX6U1AVM08AC
MCIMX6U1AVM08ACR
MCIMX6U4AVM08AB
MCIMX6U4AVM08ABR
MCIMX6U4AVM08AC

MCIMX6U4AVM08ACR
MCIMX6U5DVM10AB
MCIMX6U5DVM10ABR
MCIMX6U5DVM10AC
MCIMX6U5DVM10ACR
MCIMX6U5EVM10AB
MCIMX6U5EVM10ABR
MCIMX6U5EVM10AC
MCIMX6U5EVM10ACR
MCIMX6U6AVM08AB
MCIMX6U6AVM08ABR
MCIMX6U6AVM08AC
MCIMX6U6AVM08ACR
MCIMX6U7CVM08AB
MCIMX6U7CVM08AC
MCIMX6U8DVM10AB
MCIMX6U8DVM10AC
PCIMX6S1AVM08AC
PCIMX6S6AVM08AB
PCIMX6S6AVM08AC
PCIMX6U6AVM08AB
PCIMX6U6AVM08AC
PCIMX6U7CVM08AB
PCIMX6U8DVM08AC
PCIMX6U8DVM10AC

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AFFECTED CHANGE CATEGORIES

- DATASHEET
- DESIGN CHANGE
- ERRATA

DESCRIPTION OF CHANGE

Freescale is modifying the original PCN16548 to add orderable sample part numbers previously omitted. Due to customer response, we have now added these sample part numbers to PCN16548A. In addition, we are pleased to extend the PCN effective date to July 5, 2015.

Freescale is updating the maskset for the i.MX 6Solo/6DualLite and i.MX 6DualLite; this mask revision improves DDR timing and ROM functionality. The updated maskset will correspond to chip revision rev1.3. The final marking on the device will remain the same as the rev1.2 production devices (denoted by C on the suffix of the part number). However, for rev1.3 devices, the maskset marking on the package will change from: 2N81E >> 3N81E.

The following four errata were fixed in the 3N81E silicon revision (rev1.3):

ERR008057 MMD: Skew difference of up to 150 ps observed on SDCLK0, DQS0 and DQS7 differential traces.

ERR005768 ROM: In rare cases, secondary image boot flow may not work due to incorrect sampling of the WDOG reset.

ERR008506 ROM: Incorrect NAND Bad Block management.

ERR007926 ROM: 32 kHz internal oscillator timing inaccuracy may affect SD/MMC, NAND, and OneNAND boot

New rev5 errata has the following updates for all i.MX 6Solo/6DualLite devices:

ERR007555 PCIe: iATU Optional programmable CFG Shift feature for ECAM is not correctly updating address

ERR007556 PCIe: Core Delays Transition From L0 To Recovery After Receiving Two TS OS And Erroneous Data

ERR007557 PCIe: Extra FTS Sent When Extended Synch Bit Is Set

ERR007559 PCIe: Core Sends TS1 With Non-PAD Lane Number Too Early In Configuration.Linkwidth.Accept State

ERR007573 PCIe: Link and Lane Number-match Not Checked in Recovery

ERR007575 PCIe: LTSSM Delay When Moving From L0 To Recovery Upon Receipt of Insufficient TS1 Ordered Sets

ERR007577 PCIe: DLLP/TLP Can Be Missed on RX Path When Immediately Followed by EIOS

The updated errata revision 5 can be found at Freescale.com:

http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=i.MX6DL&fpcsp=1&tab=Documentation_Tab

An engineering bulletin detailing the hardware and software comparison between i.MX 6Solo/6DualLite silicon revisions 1.1/1.2 and 1.3 can be found at the link below using document EB804:

http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=i.MX6DL&fpcsp=1&tab=Documentation_Tab

The datasheets have been updated to revision 4 for the i.MX 6Solo/6DualLite product lines. The updated i.MX 6DualLite datasheets can be found at:

http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=i.MX6DL&fpcsp=1&tab=Documentation_Tab

The updated i.MX 6Solo revision 4 datasheets can be found at:

http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=i.MX6S&fpcsp=1&tab=Documentation_Tab

Substantive changes in the datasheets are shown below. See the revision history in the device specific datasheet for details. Some changes may not apply to certain devices depending on the capabilities supported on that device. Below are some examples of changes:

Example Orderable Part Numbers updated

Part Number Nomenclature i.MX 6Solo and 6DualLite with new rev 1.3

Modules List, UART 1 5 correction to description change

Example Part Marking for Revision 1.2/1.3 devices

Changed UARTs bullet, from up to 4.0Mbps , to up to 5.0 Mbps

Operating Ranges, changed Run mode: VDD_ARM_IN minimum value from 1.05 to 1.125V; for operation up to 396 MHz and changed LDO bypassed maximum value from 1.225V to 1.21V; for VDD_SOC_IN

Changed VDD_ARM_IN from single condition to include DualLite and Solo conditions with Maximum values

Reset Timing Parameters Removed footnote regarding SRC_POR_B rise and fall times

External Interface Module (EIM) : Changed first paragraph to describe two systems clocks used with EIM:

ACLK_EIM_SLOW_CLK_ROOT and ACLK_EXSC (for synchronous mode)

DDR I/O DDR3/DDR3L Mode AC Parameters, Added footnote about extended range for Vix
 DDR3/DDR3L Timing Parameter Table, Added DDR0, tCK(avg) and parameter values
 DDR3 Command and Address Timing Parameters change
 DDR3/DDR3L Write Cycle, symbol names of DDR17 and DDR18
 LPDDR2 Write Cycle, Changed LP21 min/max parameter values
 EIM Bus Timing Parameters, Changed footnotes regarding the system clocks
 DDR3/DDR3L Write Cycle, Changed DDR17 minimum value
 DDR3/DDR3L Write Cycle, Added footnote 4
 Electrical and Timing Information, Moved rows tSETUP[RX] and tHOLD[RX]
 21 x 21 mm Supplies Contact Assignments, Removed A1 pin
 21 x 21 mm Functional Contact Assignments, Moved rows
 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6Solo, Removed NC from A1 pin location
 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6DualLite, Removed NC from A1 pin location

Contact your Freescale or Distribution representative for product samples. See sample part numbers below.

Part ID	Sample Part
MCIMX6U5DVM10AB	KCIMX6U5EVM10AC
MCIMX6U5DVM10ABR	KCIMX6U5EVM10AC
MCIMX6U5DVM10AC	KCIMX6U5EVM10AC
MCIMX6U5DVM10ACR	KCIMX6U5EVM10AC
MCIMX6U5EVM10AB	KCIMX6U5EVM10AC
MCIMX6U5EVM10ABR	KCIMX6U5EVM10AC
MCIMX6U5EVM10AC	KCIMX6U5EVM10AC
MCIMX6U5EVM10ACR	KCIMX6U5EVM10AC
MCIMX6U7CVM08AB	KCIMX6U7CVM08AC
MCIMX6U7CVM08AC	KCIMX6U7CVM08AC
MCIMX6U8DVM10AB	KCIMX6U8DVM10AC
MCIMX6U8DVM10AC	KCIMX6U8DVM10AC
MCIMX6S5DVM10AB	KCIMX6S5EVM10AC
MCIMX6S5DVM10ABR	KCIMX6S5EVM10AC
MCIMX6S5DVM10AC	KCIMX6S5EVM10AC
MCIMX6S5DVM10ACR	KCIMX6S5EVM10AC
MCIMX6S5EVM10AB	KCIMX6S5EVM10AC
MCIMX6S5EVM10ABR	KCIMX6S5EVM10AC
MCIMX6S5EVM10AC	KCIMX6S5EVM10AC
MCIMX6S5EVM10ACR	KCIMX6S5EVM10AC
MCIMX6S7CVM08AB	KCIMX6S7CVM08AC
MCIMX6S7CVM08AC	KCIMX6S7CVM08AC
MCIMX6S8DVM10AB	KCIMX6S8DVM10AC
MCIMX6S8DVM10AC	KCIMX6S8DVM10AC
MCIMX6S1AVM08AB	KCIMX6S1AVM08AC
MCIMX6S1AVM08ABR	KCIMX6S1AVM08AC
MCIMX6S1AVM08AC	KCIMX6S1AVM08AC
MCIMX6S1AVM08ACR	KCIMX6S1AVM08AC
MCIMX6S4AVM08AB	KCIMX6S4AVM08AC
MCIMX6S4AVM08ABR	KCIMX6S4AVM08AC
MCIMX6S4AVM08AC	KCIMX6S4AVM08AC
MCIMX6S4AVM08ACR	KCIMX6S4AVM08AC
MCIMX6S6AVM08AB	KCIMX6S6AVM08AC
MCIMX6S6AVM08ABR	KCIMX6S6AVM08AC
MCIMX6S6AVM08AC	KCIMX6S6AVM08AC
MCIMX6S6AVM08ACR	KCIMX6S6AVM08AC
SCIMX6S6AVM08AB	KCIMX6S6AVM08AC
MCIMX6U1AVM08AB	KCIMX6U1AVM08AC
MCIMX6U1AVM08ABR	KCIMX6U1AVM08AC
MCIMX6U1AVM08AC	KCIMX6U1AVM08AC
MCIMX6U1AVM08ACR	KCIMX6U1AVM08AC

MCIMX6U4AVM08AB	KCIMX6U4AVM08AC
MCIMX6U4AVM08ABR	KCIMX6U4AVM08AC
MCIMX6U4AVM08AC	KCIMX6U4AVM08AC
MCIMX6U4AVM08ACR	KCIMX6U4AVM08AC
MCIMX6U6AVM08AB	KCIMX6U6AVM08AC
MCIMX6U6AVM08ABR	KCIMX6U6AVM08AC
MCIMX6U6AVM08AC	KCIMX6U6AVM08AC
MCIMX6U6AVM08ACR	KCIMX6U6AVM08AC
SCIMX6U6AVM08AB	KCIMX6U6AVM08AC

REASON FOR CHANGE

Freescale is implementing die level improvements in the DDR timing and ROM functionality, which will eliminate errata. There is an accompanying update to device marking.

ANTICIPATED IMPACT OF PRODUCT CHANGE(FORM, FIT, FUNCTION, OR RELIABILITY)

Other than intended improvements to DDR timing and ROM functionality and marking, there are no changes to form, fit, or function.

According to JEDEC Standard JESD46, lack of acknowledgement of this PCN within 30 days will be considered acceptance of change. To request further data or inquire about the notification, please enter a [Service Request](#).

For sample inquiries - please go to www.freescale.com

RELATED NOTIFICATION(S):

16548- i.MX 6DualLite and i.MX 6Solo Silicon Revision Updates

TO VIEW the GENERIC copy, click on the notification number above.

QUAL DATA AVAILABILITY DATE: 15-Jan-2015

QUALIFICATION STATUS: N/A

QUALIFICATION PLAN:

Contact Freescale Sales and Marketing for information.

RELIABILITY DATA SUMMARY:

Contact Freescale Sales and Marketing for information.

ELECTRICAL CHARACTERISTIC SUMMARY:

Contact Freescale Sales and Marketing for information.

CHANGED PART IDENTIFICATION:

The marking indicating the new revision will equal maskset 3N81E.

SAMPLE AVAILABILITY DATE: 15-Nov-2014

ATTACHMENT(S):

External attachment(s) FOR this notification can be viewed AT:

[16548A_IMX6SDLAEC_Rev4.pdf](#)

[16548A_IMX6SDLIEC_Rev4.pdf](#)

[16548A_DeQuMA_PCN_16548_20141216.pdf](#)

[16548A_IMX6SDLCE_Rev5.pdf](#)

[16548A_IMX6SDLCEC_Rev4.pdf](#)

[16548A_EB804_rev1.pdf](#)
