PRODUCT BULLETIN

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ISSUE DATE: 08-Apr-2016

NOTIFICATION: 17144

TITLE: Combined Errata Update for i.MX 6Dual/Quad and i.MX 6DualPlus/QuadPlus

EFFECTIVE DATE: 09-Apr-2016

DEVICE(S)

MPN
MCIMX6D4AVT08A
MCIMX6D4AVT08AB
MCIMX6D4AVT08AC
MCIMX6D4AVT08ACR
MCIMX6D4AVT08AD
MCIMX6D4AVT08ADR
MCIMX6D4AVT10A
MCIMX6D4AVT10AB
MCIMX6D4AVT10AC
MCIMX6D4AVT10ACR
MCIMX6D4AVT10AD
MCIMX6D4AVT10ADR
MCIMX6D5EYM10A
MCIMX6D5EYM10AC
MCIMX6D5EYM10ACR
MCIMX6D5EYM10AD
MCIMX6D5EYM10ADR
MCIMX6D5EYM10C
MCIMX6D5EYM10CC
MCIMX6D5EYM12A
MCIMX6D5EYM12AC
MCIMX6D5EYM12AD
MCIMX6D5EYM12C
MCIMX6D5EYM12CC
MCIMX6D5EZK08AD
MCIMX6D5EZK10AC
MCIMX6D5EZK10AD

MCIMX6D6AVT08A
MCIMX6D6AVT08AB
MCIMX6D6AVT08AC
MCIMX6D6AVT08ACR
MCIMX6D6AVT08AD
MCIMX6D6AVT08ADR
MCIMX6D6AVT10A
MCIMX6D6AVT10AB
MCIMX6D6AVT10AC
MCIMX6D6AVT10ACR
MCIMX6D6AVT10AD
MCIMX6D6AVT10ADR
MCIMX6D6AVT1XAD
MCIMX6D7CVT08A
MCIMX6D7CVT08AC
MCIMX6D7CVT08AD
MCIMX6D7CZK08AD
MCIMX6DP4AVT1AA
MCIMX6DP4AVT8AA
MCIMX6DP4AVT8AAR
MCIMX6DP5EYM1AA
MCIMX6DP6AVT1AA
MCIMX6DP6AVT8AA
MCIMX6DP6AVT8AAR
MCIMX6DP7CVT8AA
MCIMX6Q4AVT08A
MCIMX6Q4AVT08AB
MCIMX6Q4AVT08AC
MCIMX6Q4AVT08ACR
MCIMX6Q4AVT08AD
MCIMX6Q4AVT08ADR
MCIMX6Q4AVT10A
MCIMX6Q4AVT10AB
MCIMX6Q4AVT10AC
MCIMX6Q4AVT10ACR
MCIMX6Q4AVT10AD
MCIMX6Q4AVT10ADR
MCIMX6Q5EYM10A

MCIMX6Q5EYM10AC
MCIMX6Q5EYM10ACR
MCIMX6Q5EYM10AD
MCIMX6Q5EYM10ADR
MCIMX6Q5EYM10C
MCIMX6Q5EYM10CC
MCIMX6Q5EYM12A
MCIMX6Q5EYM12AC
MCIMX6Q5EYM12AD
MCIMX6Q5EYM12C
MCIMX6Q5EYM12CC
MCIMX6Q5EZK08AD
MCIMX6Q5EZK10AC
MCIMX6Q5EZK10AD
MCIMX6Q6AVT08A
MCIMX6Q6AVT08AB
MCIMX6Q6AVT08AC
MCIMX6Q6AVT08ACR
MCIMX6Q6AVT08AD
MCIMX6Q6AVT08ADR
MCIMX6Q6AVT10A
MCIMX6Q6AVT10AB
MCIMX6Q6AVT10AC
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MCIMX6Q6AVT10ADR
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MCIMX6Q7CVT08AC
MCIMX6Q7CVT08AD
MCIMX6Q7CZK08AD
MCIMX6QP4AVT1AA
MCIMX6QP4AVT8AA
MCIMX6QP5EYM1AA
MCIMX6QP6AVT1AA
MCIMX6QP6AVT8AA
MCIMX6QP7CVT8AA
PCIMX6D4AVT08AA
PCIMX6D5DZK10AA

PCIMX6D5EVT10AA
PCIMX6D5EVT12AA
PCIMX6D5EYM10AC
PCIMX6D5EYM10AD
PCIMX6D5EYM10CC
PCIMX6D5EYM12AC
PCIMX6D5EYM12CC
PCIMX6D6AVT10AA
PCIMX6D6AVT10AB
PCIMX6D6AVT10AC
PCIMX6D6AVT10AD
PCIMX6D7CVT08AB
PCIMX6D7CVT10AA
PCIMX6DP5EYM1AA
PCIMX6DP6AVT1AA
PCIMX6DP7CVT8AA
PCIMX6Q0AVT01A
PCIMX6Q0AYM01A
PCIMX6Q4AVT10AA
PCIMX6Q5DVT12AA
PCIMX6Q5DZK10AA
PCIMX6Q5DZK10AB
PCIMX6Q5EVT10AA
PCIMX6Q5EYM10AA
PCIMX6Q5EYM10AB
PCIMX6Q5EYM10AC
PCIMX6Q5EYM10AD
PCIMX6Q5EYM10CC
PCIMX6Q5EYM12AC
PCIMX6Q5EYM12CC
PCIMX6Q5EZK08AD
PCIMX6Q5EZK10AC
PCIMX6Q5EZK10AD
PCIMX6Q6AVT10AA
PCIMX6Q6AVT10AB
PCIMX6Q6AVT10AC
PCIMX6Q6AVT10AD
PCIMX6Q6AVT10AX

PCIMX6Q6AYM10AA
PCIMX6Q7CVT08AB
PCIMX6Q7CVT10AA
PCIMX6Q7CZK08AD
PCIMX6QP5EYM1AA
PCIMX6QP6AVT1AA
PCIMX6QP7CVT8AA
PCIMX6S5DVV10AA
PCIMX6S6AVV08A
PCIMX6U5DZT10AA
PCM2A114BBC
PCWIMX6DQ
PCWIMX6DQC
SC6Q888YM10AC
SCIMX6Q4AVT1XAD
SCIMX6Q7CZK08AD

AFFECTED CHANGE CATEGORIES

- ERRATA

DESCRIPTION OF CHANGE

The following i.MX 6 errata documentation has been updated to include additions of new errata as well as updates to existing errata. Device families related to this revision include:
i.MX 6Quad
i.MX 6Dual
i.MX 6QuadPlus
i.MX 6DualPlus

The updated errata documentation is attached to this notice and can be found at:

http://cache.nxp.com/files/32bit/doc/errata/IMX6DQCE.pdf

Additions to the errata are as follows:

ERR007926 ROM:32 kHz internal oscillator timing inaccuracy may affect SD/MMC, NAND, and OneNAND boot [i.MX 6Dual/6Quad Only]
ERR008587 PCIe: Random link down after warm reset [i.MX 6Dual/6Quad Only]
ERR009219 CCM: Asynchronous clock switching can cause unpredictable behavior [i.MX 6Dual/6Quad Only]
ERR009619 PRE: GPU3D, GPU2D and VPU cannot be power-gated if the PRE is in use [i.MX 6DualPlus/6QuadPlus Only]

ERR009623 IPU: IDMAC burst errors when crossing a 4k boundary using NI/PI 420/422 formats [i.MX 6DualPlus/6QuadPlus Only]
ERR009624 PRE: ENABLE bit cannot be set in a special case, when the EN_REPEAT bit is set [i.MX 6DualPlus/6QuadPlus Only]
ERR007555 PCIe: iATU - Optional programmable CFG Shift feature for ECAM is not correctly updating address (9000642041)
ERR007556 PCIe: Core Delays Transition From L0 To Recovery After Receiving Two TS OS And Erroneous Data (9000597455)
ERR007557 PCIe: Extra FTS sent when Extended Synch bit is set (9000588281)
ERR007559 PCIe: Core sends TS1 with non-PAD lane number too early in Configuration.Linkwidth.Accept State (9000574708)
ERR007573 PCIe: Link and lane number-match not checked in recovery (9000569433)
ERR007575 PCIe: LTSSM delay when moving from L0 to recovery upon receipt of insufficient TS1 Ordered Sets (9000514662)
ERR007577 PCIe: DLLP/TLP can be missed on RX path when immediately followed by EIOS(9000487440)
ERR007881 USB: Timeout error in Device mode
ERR008990 SSI: Channel swap in single FIFO mode when an underrun or overrun occurs
ERR009165 eCSPI: TXFIFO empty flag glitch can cause the current FIFO transfer to be sent twice
ERR009218 EIM: Signals fail to drive as outputs during boundary scan test
ERR009535 eCSPI: Burst completion by SS signal in slave mode is not functional
ERR009596 MMDC: ARCR_GUARD bits of MMDC Core AXI Re-ordering Control register (MMDC_MAARCR) doesn't behave as expected
ERR009598 SATA:SATA speed negotiation fails after suspend and resume —[i.MX 6Dual/6Quad Only]

Refer to the errata document MX6DQPCE Rev6 for more details.

REASON FOR CHANGE

The errata documentation for the following i.MX 6 products have been updated:

i.MX 6Quad
i.MX 6Dual
i.MX 6QuadPlus
i.MX 6DualPlus

ANTICIPATED IMPACT OF PRODUCT CHANGE(FORM, FIT, FUNCTION, OR RELIABILITY)

The errata describes existing conditions identified on current production devices. There are potential hardware and/or software implications to customers.

NOTE:
THE CHANGE(S) SPECIFIED IN THIS NOTIFICATION WILL BE IMPLEMENTED ON THE EFFECTIVE DATE LISTED ABOVE. To request further data or inquire about the notification, please enter a Support Case. Be aware that after you select this link to enter your request, you

must choose the topic "Product Change Notification" once on the Salesforce page.

For sample inquiries - please go to http://www.nxp.com/

QUAL DATA AVAILABILITY DATE: 28-Mar-2016

QUALIFICATION STATUS: N/A

QUALIFICATION PLAN:

N/A

RELIABILITY DATA SUMMARY:

N/A

ELECTRICAL CHARACTERISTIC SUMMARY:

N/A

CHANGED PART IDENTIFICATION:

N/A

ATTACHMENT(S):
External attachment(s) FOR this notification can be viewed AT:
17144_IMX6DQCE_.pdf
