Possible 60x Data-Bus to VCCSYN1 Noise Coupling

Detailed Description:

- On systems that implement the PLL filter at the VCCSYN1 input pin (as shown in Figure 1-1 of the attachment), it is possible for the noise from the 60x data bus switching to couple into the PLL supply voltage (VCCSYN1) internal to the MPC82xx device through the PBGA package. This issue is unique only to the VCCSYN1 input of the MPC82xx PBGA package and is more likely at high system 60x data bus frequency and heavy bus traffic, that is, high likelihood of worse case I/O buffer switching. Note that this condition has no impact on the VCCSYN input of the MPC82xx.
- When this high frequency of the 60x data bus noise is coupled onto VCCSYN1 it can cause a loss of sync between the CPU and SIU internal blocks of the MPC82xx. The failure mechanism is an instantaneous PLL jitter caused by an excessive noise on VCCSYN1 at the same time point the 60x data bus is switching.
- The recommended VCCSYN1 filter, shown in Figure 1-1 of the attachment, was designed to keep high-frequency noise from entering the chip from the VCC supply but actually works against suppressing the high frequency noise coupled onto VCCSYN1 internally. By depopulating the filter capacitors, the external supply can meet the instantaneous current requirements of the PLL circuitry and improve noise margin. If the filter capacitors are depopulated, the series resistor should be increased to 50 Ohms. This increased resistance provides better damping for the inevitable inductance in the VCCSYN1 path from board to package silicon.
- It is the recommendation of Freescale to implement the VCCSYN1 filter fix shown in Figure 1-2 of the attachment. However, system designs should still implement the filter shown in Figure 1-1 of the attachment on the VCCSYN input.