

PCN# 20150902006
F28M35x 製品チップレビジョン変更

お客様各位

今回のお知らせは、変更実施についての連絡になります。変更の詳細は、次頁以降をご参照下さい。

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以上

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Attachment: 1

本通知は、通知日前 24 ヶ月以内に本変更対象製品をご購入いただいたお客様に連絡させていただいております。変更内容詳細は下記を参照ください。

PCN 番号:	20150902006	PCN 日付:	09/10/2015
表題:	F28M35x 製品チップレビジョン変更		

PCN 詳細**変更内容:**

本通知は、Product Affected セクション記載の対象製品について、チップレビジョン及びデータシート変更を連絡するためのものです。Design 変更は、下記一覧のとおりです。

Errata Description	Errata on Die Rev B	Errata on Die Rev E
HWBIST: C28x HWBIST Should Not be Used	Yes	No
Crystal: Maximum Equivalent Series Resistance (ESR) Values are Reduced	Yes	No
XRSn may Toggle During Power Up	Yes	No
Cortex-M3 Flash: C28x Reset While C28x Holding Pump Ownership Can Cause Erroneous Cortex-M3 Flash Reads	Yes	No
Flash Pump power down: Software sequence must be followed to power down the Flash Pump	No	Yes

チップレビジョン及びデータシート番号が変更されます。

Current**New**

Die Revision	Datasheet Number	Errata	Die Revision	Datasheet Number	Errata
B	SPRS742H	SPRZ357J	E	SPRS742I	SPRZ357K

製品データシートが下記変更履歴の通り更新されます。


**TEXAS
INSTRUMENTS**
F28M35H52C, F28M35H22C, F28M35M52C, F28M35M22C, F28M35M20B, F28M35E20B
SPRS742I – JUNE 2011 – REVISED JUNE 2015
F28M35x Concerto™ Microcontrollers

Changes from February 28, 2014 to June 8, 2015 (from H Revision (FEBRUARY 2014) to I Revision)	Page
• Global: Updated temperature options.	1
• Global: The Q temperature range is available only on the F28M35H52C device.	1
• Global: Changed "CAN 2.0" to "ISO11898-1 (CAN 2.0B)"	1
• Global: Restructured document	1
• Global: Removed MICROWIRE	1
• Global: Replaced "Philips® I ² C-Bus Specification Version 2.1" with "NXP® I ² C-bus specification and user manual (UM10204)".	1
• Section 1.1 (Features): Removed "Cortex-M3 Core Hardware Built-in Self-Test" feature.	1
• Section 1.1: Updated "Controller Area Networks (CANs)" feature.	1
• Section 1.1: Added "Temperature Options" feature.	1
• Table 3-1 (Device Comparison): Updated temperature options.	7
• Table 3-1: The Q temperature range is available only on the F28M35H52C device.	7
• Table 3-1: Updated package availability.	7
• Table 3-1: Removed "Product status" row and associated footnote.	7
• Table 3-1: Added "FPU" row under "Control Subsystem — C28x"	7
• Table 3-1: Added "VCU" row under "Control Subsystem — C28x"	7
• Table 3-1: Added footnote about CAN.	9
• Table 3-1: Added footnote about EPI.	9
• Table 4-1 (Signal Descriptions): Updated DESCRIPTION of PF6_GPIO38, PG6_GPIO46, XRS, and ARS.	11
• Section 5.1 (Absolute Maximum Ratings): Moved Storage temperature (T _{stg}) from Section 5.2 to "Absolute Maximum Ratings" section.	31
• Section 5.2 (ESD Ratings): Changed section title from "Handling Ratings" to "ESD Ratings"	31
• Section 5.2: Updated section.	31
• Section 5.3 (Recommended Operating Conditions): Moved V _{IL} , V _{IH} , I _{OL} , and I _{OH} to Section 5.4	32
• Section 5.3: Updated temperature ranges.	32
• Section 5.3: Added footnote referencing the <i>Calculating Useful Lifetimes of Embedded Processors Application Report</i> (SPRABX4).	32
• Section 5.4 (Electrical Characteristics): Added V _{IL} , V _{IH} , I _{OL} , and I _{OH}	33
• Section 5.5 (Power Consumption Summary): Changed section title from "Current Consumption" to "Power Consumption Summary".	34
• Table 5-1 (Current Consumption at 150-MHz C28x SYSCLKOUT and 75-MHz M3SSCLK): Updated MAX I _{DDIO} values for SLEEP IDLE mode, SLEEP STANDBY mode, and DEEP SLEEP STANDBY mode.	34
• Section 5.8 (Timing and Switching Characteristics): Added section	40
• Section 5.8.1 (Power Sequencing): Removed "(for analog pins, this value is 0.7 V above V _{DDA})" from "There is no power sequencing requirement needed ..." paragraph.	40
• Figure 5-1 (Power-On Reset): Updated t _{W(RSL1)} . Added t _{W(RSL2)}	40
• Figure 5-1: Updated footnote about XRS pin.	40
• Table 5-5 (Reset (XRS) Timing Requirements): Updated description of t _{W(RSL2)}	41
• Table 5-6 (Reset (XRS) Switching Characteristics): t _{OSCST} : Removed MIN value of 1 ms. Changed TYP value from 10 ms to 2 ms.	41
• Section 5.8.1.1 (Power Management and Supervisory Circuit Solutions): Removed "Power Management and Supervisory Circuit Solutions" table (Table 6-17 in SPRS742H).	41
• Section 5.8.2.1 (Changing the Frequency of the Main PLL): Updated section.	42
• Table 5-9 (Crystal Oscillator Electrical Characteristics): Added table.	42
• Table 5-14 (PLL Lock Times): Updated footnote.	43
• Section 5.8.4 (Flash Timing – Master Subsystem): Removed "Master Subsystem – Flash/OTP Endurance for T Temperature Material" table (Table 6-18 in SPRS742H).	46
• Section 5.8.4: Removed "Master Subsystem – Flash/OTP Endurance for S Temperature Material" table (Table 6-19 in SPRS742H).	46
• Section 5.8.4: Removed "Master Subsystem – Flash Parameters at 75 MHz" table (Table 6-22 in SPRS742H).	46
• Section 5.8.4: Removed "Master Subsystem – Flash Parameters at 100 MHz" table (Table 6-23 in SPRS742H). ..	46
• Table 5-18 (Master Subsystem – Flash/OTP Endurance): Changed title from "Master Subsystem – Flash/OTP Endurance for Q Temperature Material" to "Master Subsystem – Flash/OTP Endurance".	46

• Table 5-18: Removed "ERASE/PROGRAM TEMPERATURE" column.	46
• Table 5-18: Removed footnote.	46
• Table 5-19 (Master Subsystem – Flash Parameters): Changed title from "Master Subsystem – Flash Parameters at 60 MHz" to "Master Subsystem – Flash Parameters".	46
• Table 5-19: Updated table.	46
• Table 5-19: Added footnotes about Program time and Erase time.	46
• Section 5.8.5 (Flash Timing – Control Subsystem): Removed "Control Subsystem – Flash/OTP Endurance for T Temperature Material" table (Table 6-27 in SPRS742H).	48
• Section 5.8.5: Removed "Control Subsystem – Flash/OTP Endurance for S Temperature Material" table (Table 6-28 in SPRS742H).	48
• Section 5.8.5: Removed "Control Subsystem – Flash Parameters at 100 MHz" table (Table 6-31 in SPRS742H). ..	48
• Section 5.8.5: Removed "Control Subsystem – Flash Parameters at 150 MHz" table (Table 6-32 in SPRS742H). ..	48
• Table 5-23 (Control Subsystem – Flash/OTP Endurance): Changed title from "Control Subsystem – Flash/OTP Endurance for Q Temperature Material" to "Control Subsystem – Flash/OTP Endurance".	48
• Table 5-23: Removed "ERASE/PROGRAM TEMPERATURE" column.	48
• Table 5-23: Removed footnote.	48
• Table 5-24 (Control Subsystem – Flash Parameters): Changed title from "Control Subsystem – Flash Parameters at 60 MHz" to "Control Subsystem – Flash Parameters".	48
• Table 5-24: Updated table.	48
• Table 5-24: Added footnotes about Program time and Erase time.	48
• Section 5.10.4 (Cortex-M3 Controller Area Network): Added NOTE about CAN and D_CAN.	106
• Section 6 (Detailed Description): Changed section title from "Device Overview" to "Detailed Description".	150
• Table 6-2 (Control Subsystem Peripheral Frame 0): Changed title from "Control Subsystem Peripheral Frame 0 (Includes Analog)" to "Control Subsystem Peripheral Frame 0".	151
• Table 6-2: 0000 1780 – 0000 17FF: Changed register name from "C Hardware Logic BIST Registers" to "Hardware BIST Registers".	151
• Table 6-10 (Master Subsystem Peripherals): 400F B000 – 400F B1FF: Changed "PBIST Control Registers" to "Reserved".	158
• Table 6-10: 400F BB00 – 400F BBFF: Changed "M HWBIST Registers" to "Reserved".	158
• Section 6.2 (Master Subsystem): Removed "Cortex-M3 Core Hardware Built-In Self-Test" section (Section 3.3.2 in SPRS742H).	161
• Table 6-13 (Interrupts from NVIC to Cortex-M3): Interrupt Number 91: Changed "PBIST Done" to "Reserved".	163
• Section 6.3.2 (C28x Core Hardware Built-In Self-Test): Updated section.	169
• Section 6.8.3 (Analog and Digital Subsystems' Power-On-Reset Functionality): Added statement clarifying that POR is always enabled.	183
• Figure 6-7 (Connecting Input Clocks to a Concerto Device): Updated figure	184
• Section 6.9.3 (External Oscillators (Pins X1 and XCLKIN)): Updated section.	185
• Section 6.9.4 (Main PLL): Changed the maximum Main PLL output clock from 550 MHz to 300 MHz.	185
• Figure 6-8 (Main PLL): Changed the maximum Main PLL output clock from 550 MHz to 300 MHz.	186
• Section 6.11.3 (C28x STANDBY Mode): Changed MTOCIPCINT1 to MTOCIPCINT2	201
• Section 6.15.2 (GPIO_MUX2): Replaced "GPG" with "GPE" (for example, replaced "GPGMUX1" with "GPEMUX1". Replaced "register set G" with "register set E".	216
• Figure 6-17 (Pin Muxing on AIO_MUX1, AIO_MUX2, and GPIO_MUX2): Replaced "GPG" with "GPE".	217
• Figure 7-1 (Device Nomenclature): Updated TEMPERATURE RANGE.	227
• Section 7.2 (Documentation Support): Added reference documents	228

変更されたデータシートは下記のリンクより入手可能です。

<http://www.ti.com/lit/ds/symlink/f28m35h52c.pdf>

変更理由：

製品 performance 改善

外観, 寸法, 機能, 品質, 信頼性(positive / negative)に関する懸念事項：

なし

注記)

1. 本資料は英語原文(一部)の日本語訳になりますが、TI の公式文書はあくまで英語原文になります。英語原文と日本語訳に齟齬がある場合には、英語原文が優先されます。
2. 上記項目以外、本資料に日本語訳が記載されていない項目については英語原文を参照ください。

原文のみ記載の項目例：

- **Proposed 1st Ship Date** (変更品出荷開始予定日)
- **Last date to order/Last date to ship** (最終受注日/最終出荷日)
- **Estimated Sample Availability** (サンプル入手可能予定時期)
- **Change Type** (変更項目タイプ)
- **Anticipated impact on Material Declaration** (材料宣言に関する懸念事項)
- **Changes to product identification resulting from this PCN** (本変更による製品識別の変更)
- **Product Affected** (対象製品)
- **Qualification Data** (認定試験データ)
- **Appendix** (付属資料) 等