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お客様各位

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データシート訂正（UCC1895/2895/3895 製品）のご案内

拝啓 貴社益々ご清栄の事とお喜び申し上げます。平素は弊社製品のご愛顧を賜り、厚く御礼申し上げます。さて、標題の件につきまして下記にご連絡させていただきます。ご査収の程、宜しくお願い申し上げます。

敬具

－ 記 －

通知タイプ	☐Initial notice (Plan)	■Final notice		
変更概要	■Design/Specification	☐Design	■Electrical	☐Mechanical
	Wafer Fab	☐Site	☐Process	☐Material
	Wafer Bump	☐Site	☐Process	☐Material
	Assembly	☐Site	☐Process	☐Material
	Test	☐Site	☐Process	
	Others	☐Packing/Shipping/Labeling	☐ -	
変更内容	データシート 10 項目の記載訂正 現行 ：10 項目の記載 変更後：10 項目の記載訂正			
対象製品	対象製品リスト参照			
変更時期	データシート訂正は 8 月下旬に実施済みです。			
品質認定試験	☐計画	☐終了		
製品表示	■変更無し	☐変更あり		
備考	—			

尚、ご不明な点、ご質問等がございましたら、担当営業或いはpcn_tij@list.ti.comにお問い合わせ下さい。

以上

変更内容

内容：今回のお知らせは、通知のみを目的としたものになります。
発行済みのデータシートに訂正箇所がありその訂正をお知らせするものです。弊社 HPA(ハイパフォーマンスアナログ) ″ UCC1895/2895/3895 ″製品について、製品の変更は一切ありませんが、製品特性をより反映する為にデータシートの記載訂正を実施しました。更新済のデータシートについては、下記webを参照ください。尚、今回の変更で訂正対象項目を除き、製品についての互換性(寸法/交差), 外観, 品質, 信頼性への影響はありません。

理由：データシートの訂正の為

対象製品リスト

対象製品名				
UCC1895J	UCC2895DWTR	UCC2895N	UCC2895QG3	UCC3895PW
UCC1895J883B	UCC2895DWTR/1	UCC2895NG4	UCC3895DW	UCC3895PWG4
UCC1895L	UCC2895DWTR/1G4	UCC2895PW	UCC3895DWG4	UCC3895PWTR
UCC2895DW	UCC2895DWTR/3	UCC2895PWG4	UCC3895DWTR	UCC3895PWTRG4
UCC2895DW/1	UCC2895DWTR/3G4	UCC2895PWTR	UCC3895DWTRG4	UCC3895Q
UCC2895DWG4	UCC2895DWTRG4	UCC2895PWTRG4	UCC3895N	UCC3895QG3
UCC2895DWR/3	UCC2895MDWREP	UCC2895Q	UCC3895NG4	

詳細：

1. Datasheet#　　SLUS157K ⇒　　SLUS157L
http://focus.ti.com/lit/ds/symlink/ucc1895.pdf

Item	Page/Location	Description of Change
C.1	Pg. 3, Title Heading, RECOMMENDED OPERATING CONDITIONS table	Added explanatory note (3)
C.2	Pg. 3, Supply voltage bypass capacitor, V_{DD}, RECOMMENDED OPERATING CONDITIONS table	Change, TYPICAL spec from 0.1 to 10 x Cref. Also added explanatory note (1).
C.3	Pg. 3, Reference bypass capacitor C_{REF}, RECOMMENDED OPERATING CONDITIONS table	Remove typical spec of 0.1 and add MIN spec of 0.1. Also added explanatory note (2).
C.4	Pg. 3, Delay resistor R_{DEL_AB}, R_{DEL_CD}, RECOMMENDED OPERATING CONDITIONS table	Change, units from pF to kΩ
C.5	Pg. 3, Operating junction temperature, TJ	Added explanatory note (4)
C.6	Pg. 4, V_{IH_SYNC}, “ELECTRICAL CHARACTERISTICS” table	Change parameter description from “High-level input voltage, SYNC” to “SYNC input threshold, SYNC”
C.7	Pg. 4, V_{OH_SYNC}, “ELECTRICAL CHARACTERISTICS” table	Change parameter description from “High-level input voltage, SYNC” to “High-level output voltage, SYNC”
C.8	Pg. 4, V_{OH_SYNC}, “ELECTRICAL CHARACTERISTICS” table	Change test conditions from “V_{CT} = 2.6 V” to “VCT = 0.0 V”
C.9	Pg. 6, VDD, “TERMINAL FUNCTIONS” table	Added last sentence, “The addition of a 10−µF low ESR, low ESL between VDD and PGND is recommended.”
C.10	Pg. 11, Chip supply (VDD), “DETAILED PIN DESCRIPTION section	Added last sentence, “The addition of a 10−µF low ESR, low ESL between VDD and PGND is recommended.

C.1 Pg. 3, Title Heading, RECOMMENDED OPERATING CONDITIONS table
C.2 Pg. 3, Supply voltage bypass capacitor, VDD, RECOMMENDED OPERATING CONDITIONS table
C.3 Pg. 3, Reference bypass capacitor CREF, RECOMMENDED OPERATING CONDITIONS table
C.4 Pg. 3, Delay resistor RDEL_AB, RDEL_CD, RECOMMENDED OPERATING CONDITIONS table
C.5 Pg. 3, Operating junction temperature, TJ

RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
Supply voltage, V_{DD}	9		16.5	V
Supply voltage bypass capacitor, V_{DD}		0.1		µF
Reference bypass capacitor, C_{REF}		0.1	1.0	
Timing capacitor, C_T (for 500 kHz switching frequency)		220		pF
Timing resistor, R_T (for 500 kHz switching frequency)		82		kΩ
Delay resistor R_{DEL_AB}, R_{DEL_CD}	2.5		40	pF
Operating junction temperature, T_J(3)	−55		125	°C

(3) It is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

RECOMMENDED OPERATING CONDITIONS(3)

	MIN	TYP	MAX	UNIT
Supply voltage, V_{DD}	9		16.5	V
Supply voltage bypass capacitor, V_{DD}(1)		10 x C_{REF}		µF
Reference bypass capacitor, C_{REF}(2)	0.1		1.0	
Timing capacitor, C_T (for 500 kHz switching frequency)		220		pF
Timing resistor, R_T (for 500 kHz switching frequency)		82		kΩ
Delay resistor R_{DEL_AB}, R_{DEL_CD}	2.5		40	
Operating junction temperature, T_J(4)	−55		125	°C

(1) The V_{DD} capacitor should be a low ESR, ESL ceramic capacitor located directly across the VDD and PGND pins. A larger bulk capacitor s hould belocated as physically close as possible to the V_{DD} pins.
(2) The V_{REF} capacitor should be a low ESR, ESL ceramic capacitor located directly across the REF and GND pins. If a larger capacitor is d esired for the V_{REF} then it should be located near the V_{REF} cap and connected to the V_{REF} pin with a resistor of 51 Ω or greater. The bulk capacitor on V_{DD} must be a factor of 10 greater than the total V_{REF} capacitance.
(3) It is recommended that there be a single point grounded between GND and PGND directly under the device. There should be a seperate ground plane associated with the GND pin and all components associated with pins 1 through 12 plus 19 and 20 be located over this gnd plane. Any connections associated with these pins to ground should be connected to this ground plane
(4) It is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

C.6 Pg. 4, VIH_SYNC,"ELECTRICAL CHARACTERISTICS" table
C.7 Pg. 4, VOH_SYNC, "ELECTRICAL CHARACTERISTICS" table
C.8 Pg. 4, VOH_SYNC, "ELECTRICAL CHARACTERISTICS" table

ELECTRICAL CHARACTERISTICS V_{DD} = 12 V, R_T = 82 kΩ, C_T = 220 pF, R_{DELAB} = 10 kΩ, R_{DELCD} = 10 kΩ, C_{REF} = 0.1 µF, C_{VDD} = 0.1 µF and no load on the outputs, $T_A = T_J$. T_A = 0°C to 70°C for UCC3895x, T_A = −40°C to 85°C for UCC2895x and TA = −55°C to 125°C for the UCC1895x. (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
OSCILLATOR							
V_{IH_SYNC}	High-level input voltage, SYNC			2.05	2.10	2.40	V
V_{OH_SYNC}	High-level input voltage, SYNC	I_{SYNC} = −400 µA,	V_{CT} = 2.6 V	4.1	4.5	5.0	
V_{OL_SYNC}	Low-level output voltage, SYNC	I_{SYNC} = 100 µA,	V_{CT} = 2.6 V	0.0	0.5	1.0	

ELECTRICAL CHARACTERISTICS V_{DD} = 12 V, R_T = 82 kΩ, C_T = 220 pF, R_{DELAB} = 10 kΩ, R_{DELCD} = 10 kΩ, C_{REF} = 0.1 µF, C_{VDD} = 0.1 µF and no load on the outputs, $T_A = T_J$. T_A = 0°C to 70°C for UCC3895x, T_A = −40°C to 85°C for UCC2895x and TA = −55°C to 125°C for the UCC1895x. (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
OSCILLATOR							
V_{IH_SYNC}	SYNC input threshold, SYNC			2.05	2.10	2.40	V
V_{OH_SYNC}	High-level output voltage, SYNC	I_{SYNC} = −400 µA,	V_{CT} = 2.6 V	4.1	4.5	5.0	
V_{OL_SYNC}	Low-level output voltage, SYNC	I_{SYNC} = 100 µA,	V_{CT} = 0.0 V	0.0	0.5	1.0	

C.9 Pg. 6, VDD, “TERMINAL FUNCTIONS” table

TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
VDD	15	I	Power supply input pin. VDD must be bypassed with a minimum of a 1.0µF low ESR, low ESL capacitor to ground.

TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
VDD	15	I	Power supply input pin. VDD must be bypassed with a minimum of a 1.0µF low ESR, low ESL capacitor to ground. The addition of a 10-µF low ESR, low ESL between VDD and PGND is recommended.

C.10 Pg. 11, Chip supply (VDD), “DETAILED PIN DESCRIPTION sectionDESCRIPTION section

Chip Supply (VDD)

This is the input pin to the chip. VDD must be bypassed with a minimum of 1.0µF low ESR, low ESL capacitor to ground.

Chip Supply (VDD)

This is the input pin to the chip. VDD must be bypassed with a minimum of 1.0µF low ESR, low ESL capacitor to ground. The addition of a 10-µF low ESR, low ESL between VDD and PGND is recommended.