日本テキサス・インスツルメンツ株式会社

本社：〒160-8366
東京都新宿区西新宿 6 丁目 24 番 1 号
西新宿三井ビルディング

報告書番号 ： PCN#20091211000
2010 年 1 月 15 日

お客様各位

日本テキサス・インスツルメンツ株式会社
営業・技術本部 カスタマドキュメント
マネージャ 牧 達郎

データシート訂正(TPS65023 製品)のご案内

拝啓 貴社益々ご清栄の事とお喜び申し上げます。平素は弊社製品のご愛顧を賜り、厚く御礼申し上げます。さて、標題の件につきまして下記にご連絡させていただきます。ご査収の程、宜しくお願い申し上げます。

敬具

― 記 ―

通知タイプ	☐Initial notice (Plan)	■Final notice		
変更概要	■Design/Specification	☐Design	■Electrical	☐Mechanical
	Wafer Fab	☐Site	☐Process	☐Material
	Wafer Bump	☐Site	☐Process	☐Material
	Assembly	☐Site	☐Process	☐Material
	Test	☐Site	☐Process	
	Others	☐Packing/Shipping/Labeling	☐ -	
変更内容	データシート 14 項目の記載訂正 現行 ：14 項目の記載 変更後：14 項目の記載訂正			
対象製品	対象製品リスト参照			
変更時期	データシート訂正は 1 月上旬に実施済みです。 4 月下旬の出荷より予定しています。			
品質認定試験	☐計画	☐終了		
製品表示	■変更無し	☐変更あり		
備考	―			

尚、ご不明な点、ご質問等がございましたら、担当営業或いはpcn_tij@list.ti.comにお問い合わせ下さい。

以上

変更内容

内容：発行済みのデータシートに訂正箇所がありその訂正をお知らせするものです。弊社 PWR(パワーマネジメント) TPS65023製品について、製品の変更は一切ありませんが、製品特性をより反映する為にデータシートの記載訂正を実施しました。尚、今回の変更で訂正対象項目を除き、製品についての互換性(寸法/公差),外観,動作特性,品質,信頼性への影響はありません。

理由：製品特性をより反映する為

対象製品リスト

対象製品名			
TPS65023RSBR	TPS65023RSBRG4	TPS65023RSBT	TPS65023RSBTG4

詳細：

1. Datasheet#　TPS65023　SLVS670G ⇒ SLVS670H
http://focus.ti.com/lit/ds/symlink/tps65023.pdf

Item	Page/Location	Description of Change
C.1	Pg 2, RECOMMENDED OPERATING CONDITIONS	Changed IO(DCDC1) MAX from 1500 mA to 1700 mA
C.2	Pg 3, RECOMMENDED OPERATING CONDITIONS	Added High level input voltage for the SDAT pin
C.3	Pg 6, ELECTRICAL CHARACTERISTICS	Changed IO from 1500 mA MIN to 1700 mA
C.4	Pg 6, ELECTRICAL CHARACTERISTICS	Changed IO maximum from 1.5 A to 1.7 A for VDCDC1 fixed and adjustable output voltage test condition specs.
C.5	Pg 6, ELECTRICAL CHARACTERISTICS	Changed IO maximum from 1500 mA to 1700 mA for VDCDC1 Load Regulation test condition
C.6	Pg 6, ELECTRICAL CHARACTERISTICS	Changed VDCDC1 "Soft start ramp time" spec to "tStart and tRamp" spec with MIN TYP MAX values.
C.7	Pg 7, ELECTRICAL CHARACTERISTICS	Changed VDCDC2 "Soft start ramp time" spec To "tStart and tRamp" spec with MIN TYP MAX values.
C.8	Pg 8, ELECTRICAL CHARACTERISTICS	Changed VDCDC3 "Soft start ramp time" spec To "tStart and tRamp" spec with MIN TYP MAX values.
C.9	Pg 12, FUNCTIONAL BLOCK DIAGRAM	Changed FBD graphic to show 1700 mA for DCDC1 Buck Converter
C.10	Pg 21, DETAILED DESCRIPTION	Changed text string from "1.2 V or 1.8 V" to "1.2 V or 1.6 V" in the STEP-DOWN CONVERTERS, VDCDC1 description.
C.11	Pg 30, SERIAL INTERFACE DESCRIPTION	Changed th(DATA) MIN spec from 0 ns to 300 ns
C.12	Pg 30, SERIAL INTERFACE DESCRIPTION	Changed tsu(DATA) MIN spec from 100 ns to 300 ns
C.13	Pg 41, APPLICATION INFORMATION	Changed graphic entity to the one used in the Application Note SLVA273
C.14	Pg 44, REVISION HISTORY	Added change summary from Datasheet Rev.G to Rev.H

C1 Pg 2 RECOMMENDED OPERATING CONDITIONS

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$I_{O(DCDC1)}$	Output current at L1			1500	mA
	Inductor at L1 (2)	1.5	2.2		µH

(2) See *Applications Information* section for more information.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$I_{O(DCDC1)}$	Output current at L1			1700	mA
	Inductor at L1 (2)	1.5	2.2		µH

(2) See *Applications Information* section for more information.

C2 Pg 3 RECOMMENDED OPERATING CONDITIONS

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL SIGNALS : SCLK, SDAT (input), DCDC1_EN, DCDC2_EN, DCDC3_EN, LDO_EN, DEFLDO1, DEFLDO2						
V_{IH}	High level input voltage	Resistor pullup at SCLK and SDAT = 4.7 kΩ, pulled to VRTC	1.3		VCC	V
V_{IL}	Low level input voltage	Resistor pullup at SCLK and SDAT = 4.7 kΩ, pulled to VRTC	0		0.4	V

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL SIGNALS : SCLK, SDAT (input), DCDC1_EN, DCDC2_EN, DCDC3_EN, LDO_EN, DEFLDO1, DEFLDO2						
V_{IH}	High level input voltage (except the SDAT pin)	Resistor pullup at SCLK = 4.7 kΩ, pulled to VRTC	1.3		V_{CC}	V
V_{IH}	High level input voltage for the SDAT pin	Resistor pullup at SDAT = 4.7 kΩ, pulled to VRTC	1.45		V_{CC}	V
V_{IL}	Low level input voltage	Resistor pullup at SCLK and SDAT = 4.7 kΩ, pulled to VRTC	0		0.4	V

C3-6 Pg 6 ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDCDC1 STEP-DOWN CONVERTER							
I_O	Maximum output current			1500			mA
	Fixed output voltage FPWMDCDC1=0	All VDCDC1	VINDCDC1 = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 1.5 A	–2		2	%
	Fixed output voltage FPWMDCDC1=1	All VDCDC1	VINDCDC1 = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 1.5 A	–1		1	%
	Adjustable output voltage with resistor divider at DEFDCDC1; FPWMDCDC1=0		VINDCDC1 = VDCDC1 + 0.3 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 1.2 A	–2		2	%
	Adjustable output voltage with resistor divider at DEFDCDC1; FPWMDCDC1=1		VINDCDC1 = VDCDC1 + 0.3 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 1.2 A	–1		1	%
	Load Regulation		I_O = 10 mA to 1200 mA		0.25		%/A
	Soft start ramp time		VDCDC1 ramping from 5% to 95% of target value		750		µs

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDCDC1 STEP-DOWN CONVERTER							
I_O	Maximum output current			1700			mA
	Fixed output voltage FPWMDCDC1=0	All VDCDC1	VINDCDC1 = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 1.7 A	–2		2	%
	Fixed output voltage FPWMDCDC1=1	All VDCDC1	VINDCDC1 = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 1.7 A	–1		1	%
	Adjustable output voltage with resistor divider at DEFDCDC1; FPWMDCDC1=0		VINDCDC1 = VDCDC1 + 0.5 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 1.7 A	–2		2	%
	Adjustable output voltage with resistor divider at DEFDCDC1; FPWMDCDC1=1		VINDCDC1 = VDCDC1 + 0.5 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 1.7 A	–1		1	%
	Load Regulation		I_O = 10 mA to 1700 mA		0.25		%/A
t_{Start}	Start-up time		Time from active EN to start switching	145	175	200	µs
t_{Ramp}	V_{OUT} ramp-up time		Time to ramp from 5% to 95% of V_{OUT}	400	750	1000	µs

C7 Pg 7 ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Soft start ramp time	VDCDC2 ramping from 5% to 95% of target value		750		µs

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{Start}	Start-up time	Time from active EN to start switching	145	175	200	µs
t_{Ramp}	V_{OUT} ramp-up time	Time to ramp from 5% to 95% of V_{OUT}	400	750	1000	µs

C8 Pg 8 ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Soft start ramp time	VDCDC3 ramping from 5% to 95% of target value		750		µs

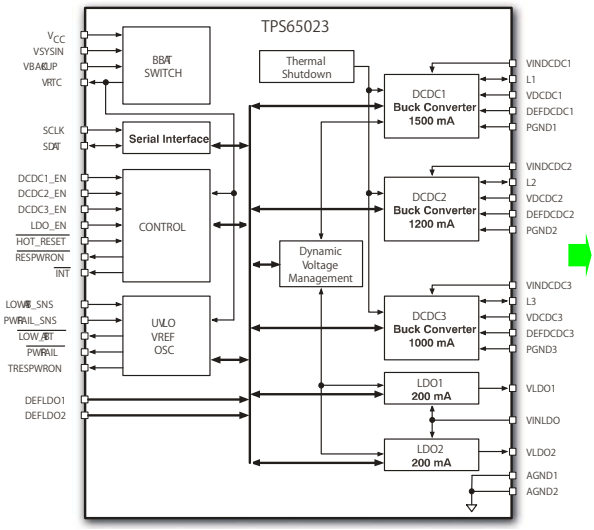
ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

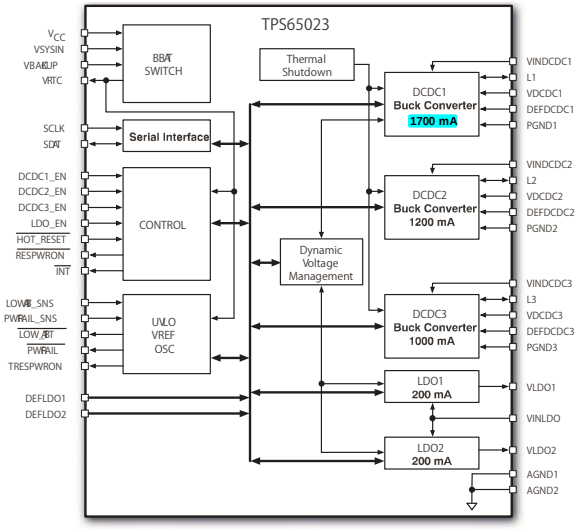
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{Start}	Start-up time	Time from active EN to start switching	145	175	200	µs
t_{Ramp}	V_{OUT} ramp-up time	Time to ramp from 5% to 95% of V_{OUT}	400	750	1000	µs

C9 Pg 12 FUNCTIONAL BLOCK DIAGRAM

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



C10 Pg 21 DETAILED DESCRIPTION.

The converter output voltages can be programmed via the DEFDCDC1, DEFDCDC2 and DEFDCDC3 pins. The pins can either be connected to GND, VCC, or to a resistor divider between the output voltage and GND. The VDCDC1 converter defaults to 1.2 V or 1.8 V depending on the DEFDCDC1 configuration pin. If DEFDCDC1 is tied to ground, the default is 1.2 V. If it is tied to VCC, the default is 1.8 V. When the DEFDCDC1 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to VINDCDC1 V. See the application information section for more details. The core voltage can be reprogrammed via the serial interface in the range of 0.8 V to 1.6 V with a programmable slew rate. The converter is forced into PWM operation whilst any programmed voltage change is underway, whether the voltage is being increased or decreased. The DEFCORE and DEFSLEW registers are used to program the output voltage and slew rate during voltage transitions.

The converter output voltages can be programmed via the DEFDCDC1, DEFDCDC2 and DEFDCDC3 pins. The pins can either be connected to GND, VCC, or to a resistor divider between the output voltage and GND. The VDCDC1 converter defaults to 1.2 V or 1.6 V depending on the DEFDCDC1 configuration pin. If DEFDCDC1 is tied to ground, the default is 1.2 V. If it is tied to VCC, the default is 1.6 V. When the DEFDCDC1 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to VINDCDC1 V. See the application information section for more details. The core voltage can be reprogrammed via the serial interface in the range of 0.8 V to 1.6 V with a programmable slew rate. The converter is forced into PWM operation whilst any programmed voltage change is underway, whether the voltage is being increased or decreased. The DEFCORE and DEFSLEW registers are used to program the output voltage and slew rate during voltage

C11-12 Pg 30 SERIAL INTERFACE DESCRIPTION

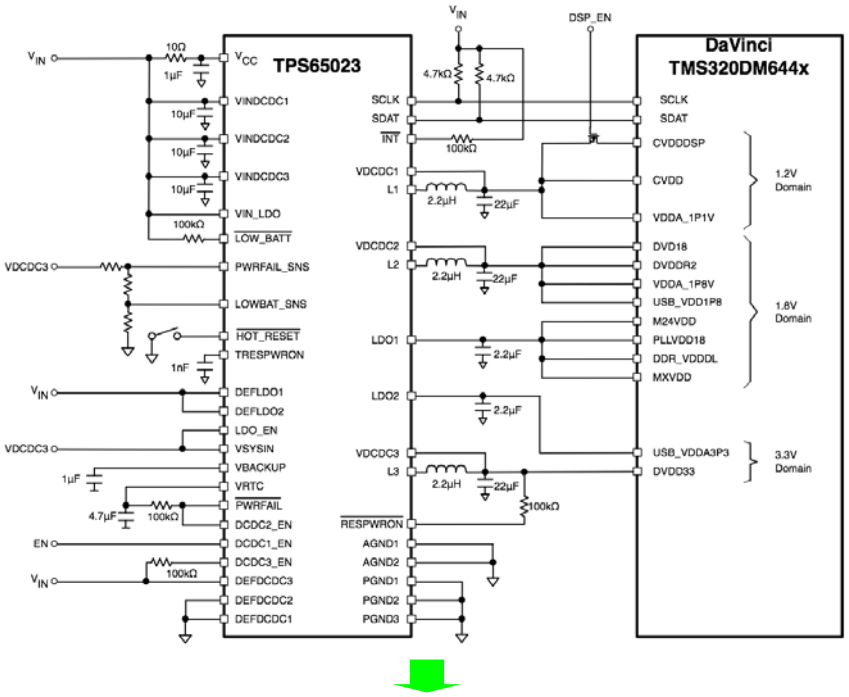
		MIN	MAX	UNIT
$t_{h(DATA)}$	Data input hold time	0		ns
$t_{su(DATA)}$	Data input setup time	100		ns

		MIN	MAX	UNIT
$t_{h(DATA)}$	Data input hold time	300		ns
$t_{su(DATA)}$	Data input setup time	300		ns

C13 Pg 41 APPLICATION INFORMATION

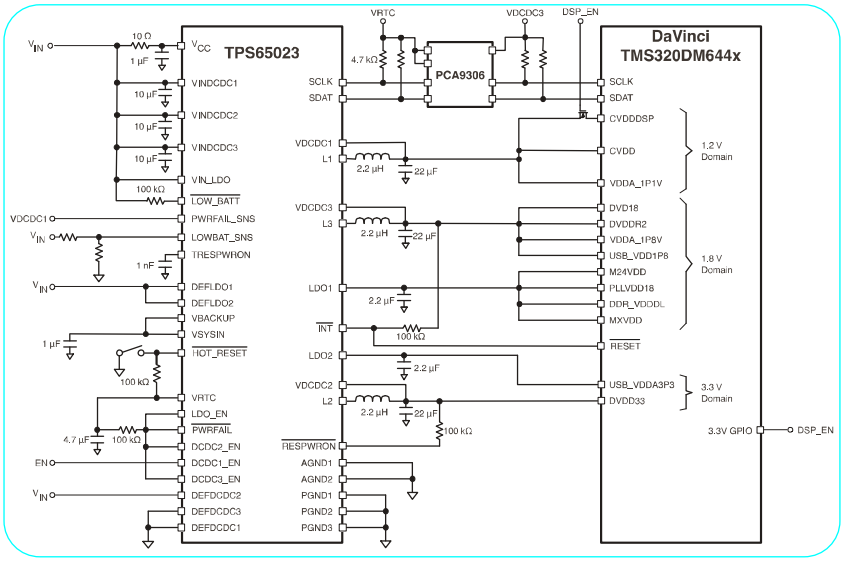
APPLICATION INFORMATION

Typical Configuration for the Texas Instruments® TMS320DM644x DaVinci Processors



APPLICATION INFORMATION

Typical Configuration for the Texas Instruments® TMS320DM644x DaVinci Processors



C14 Pg 44, REVISION HISTORY

Changes from Revision G (October 2008) to Revision H	Page
• Changed $I_{O(DCDC1)}$ MAX from: 1500 mA to: 1700 mA	2
• Added High level input voltage for the SDAT pin	3
• Changed I_O from:1500 mA MIN to 1700 mA	6
• Changed I_O maximum from:1.5 A to: 1.7 A for VDCDC1 fixed and adjustable output voltage test condition specs.	6
• Changed I_O maximum from: 1500 mA to: 1700 mA for VDCDC1 Load Regulation test condition	6
• Changed VDCDC1 "Soft start ramp time" spec to: "t_{Start} and t_{Ramp}" specifications with MIN TYP MAX values.	6
• Changed VDCDC2 "Soft start ramp time" spec To: "t_{Start} and t_{Ramp}" specifications with MIN TYP MAX values.	7
• Changed VDCDC3 "Soft start ramp time" spec To: "t_{Start} and t_{Ramp}" specifications with MIN TYP MAX values.	8
• Changed FBD graphic to show 1700 mA for DCDC1 Buck Converter	12
• Changed text string from: "1.2 V or 1.8 V" to: "1.2 V to 1.6 V" in the STEP-DOWN CONVERTERS.,VDCDC1.... description.	21
• Changed $t_{h(DATA)}$ MIN spec from 0 ns to 300 ns	30
• Changed $t_{su(DATA)}$ MIN spec from 100 ns to 300 ns	30
• Changed graphic entity to the one used in the Application Note SLVA273	41