日本テキサス・インスツルメンツ株式会社

本社：〒160-8366
東京都新宿区西新宿 6 丁目 24 番 1 号
西新宿三井ビルディング

報告書番号 ： PCN#20100308003
2010 年 3 月 17 日

お客様各位

日本テキサス・インスツルメンツ株式会社
営業・技術本部 カスタマドキュメント
マネージャ 牧 達郎

データシート訂正(TPS704xx製品)のご案内

拝啓 貴社益々ご清栄の事とお喜び申し上げます。平素は弊社製品のご愛顧を賜り、厚く御礼申し上げます。さて、標題の件につきまして下記にご連絡させていただきます。ご査収の程、宜しくお願い申し上げます。

敬具

－ 記 －

| | | | | |
|---|---|---|---|---|
| 通知タイプ | ☐Initial notice (Plan) | ■Final notice | | |
| 変更概要 | ■Design/Specification | ☐Design | ■Electrical | ☐Mechanical |
| | Wafer Fab | ☐Site | ☐Process | ☐Material |
| | Wafer Bump | ☐Site | ☐Process | ☐Material |
| | Assembly | ☐Site | ☐Process | ☐Material |
| | Test | ☐Site | ☐Process | |
| | Others | ☐Packing/Shipping/Labeling | ☐ - | |
| 変更内容 | データシート 6 項目の記載訂正<br>現行 ：6 項目の記載<br>変更後：6 項目の記載訂正 | | | |
| 対象製品 | 対象製品リスト参照 | | | |
| 変更時期 | データシート訂正は 3 月上旬に実施済みです。 | | | |
| 品質認定試験 | ☐計画 | ☐終了 | | |
| 製品表示 | ■変更無し | ☐変更あり | | |
| 備考 | — | | | |

尚、ご不明な点、ご質問等がございましたら、担当営業或いはpcn_tij@list.ti.comにお問い合わせ下さい。

以上

# 変更内容

内容：今回のお知らせは、通知のみを目的としたものになります。
発行済みのデータシートに訂正箇所がありその訂正をお知らせするものです。弊社 PWR(パワーマネジメント) TPS704xx製品について、製品の変更は一切ありませんが、製品特性をより反映する為にデータシートの記載訂正を実施しました。尚、今回の変更で訂正対象項目を除き、製品についての互換性(寸法/公差),外観,動作特性,品質,信頼性への影響はありません。

理由：製品特性をより反映する為

## 対象製品リスト

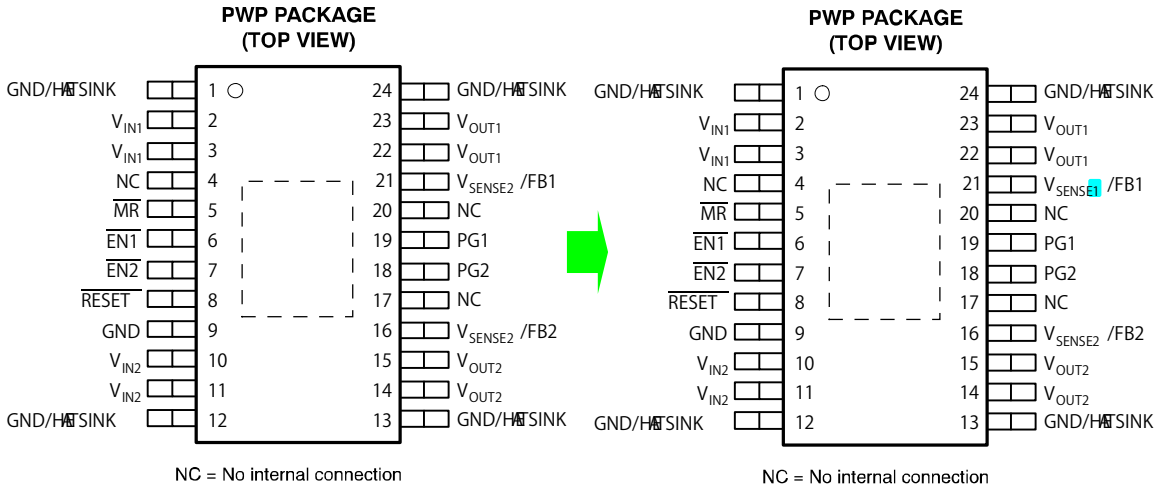
| 対象製品名 | | | | |
|---|---|---|---|---|
| TPS70402PWP | TPS70445PWP | TPS70448PWP | TPS70451PWP | TPS70458PWP |
| TPS70402PWPG4 | TPS70445PWPG4 | TPS70448PWPG4 | TPS70451PWPG4 | TPS70458PWPG4 |
| TPS70402PWPR | TPS70445PWPR | TPS70448PWPR | TPS70451PWPR | TPS70458PWPR |
| TPS70402PWPRG4 | TPS70445PWPRG4 | TPS70448PWPRG4 | TPS70451PWPRG4 | TPS70458PWPRG4 |

詳細：

1. Datasheet#　　TPS704xx　　SLVS307D ⇒　　SLVS307E
http://focus.ti.com/lit/ds/symlink/tps70445.pdf

| Item | Page/Location | Description of Change |
|---|---|---|
| C.1 | Pg 1,<br>PINOUT DRAWING | Corrected pin description for pin 21 in pinout drawing |
| C.2 | Pg 4,<br>DISSIPATION RATINGS | Updated Dissipation Ratings table values |
| C.3 | Pg 6,<br>ELECTRICAL CHARACTERISTICS | Deleted falling edge delay specification |
| C.4 | Pg 7,<br>Fixed Voltage Version | Updated Fixed Voltage Version block diagram |
| C.5 | Pg 8,<br>Adjustable Voltage Version | Updated Adjustable Voltage Version block diagram |
| C.2 | Pg 32,<br>REVISION HISTORY | Added change summary from Datasheet Rev. D to Rev. E |

### C.1 Pg 1,PINOUT DRAWING



## C.2 Pg 4,DISSIPATION RATINGS

### DISSIPATION RATINGS

| PACKAGE | AIR FLOW (CFM) | $T_A \le +25°C$ | DERATING FACTOR | $T_A = +70°C$ | $T_A = +85°C$ |
|---|---|---|---|---|---|
| PWP (1) | 0 | 3.32 W | 33.2 mW/°C | 1.83 W | 1.33 W |
| | 250 | 4.58 W | 45.87 mW/°C | 2.52 W | 1.83 W |

(1) This parameter is measured with the recommended copper heat sink pattern on a 4-layer PCB, 1 oz. copper on a 4-in by 4-in ground layer. Simultaneous and continuous operation of both regulator outputs at full load may exceed the power dissipation rating of the PWP package. For more information, refer to TI technical brief SLMA002.

### DISSIPATION RATINGS

| PACKAGE | AIR FLOW (CFM) | $T_A \le +25°C$ | DERATING FACTOR | $T_A = +70°C$ | $T_A = +85°C$ |
|---|---|---|---|---|---|
| PWP (1) | 0 | 3.067W | 30.67mW/°C | 1.687W | 1.227W |
| | 250 | 4.115W | 41.15mW/°C | 2.265W | 1.646W |

(1) This parameter is measured with the recommended copper heat sink pattern on a 4-layer PCB, 1 oz. copper on a 4-in by 4-in ground layer. For more information, refer to TI technical brief SLMA002.

## C.3 Pg 6,ELECTRICAL CHARACTERISTICS (continued)

### ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating junction temperature range ($T_J$ = –40°C to +125°C), $V_{IN1}$ or $V_{IN2}$ = $V_{OUT(nom)}$ + 1 V, $I_O$ = 1 mA, $\overline{EN}$ = 0 V, $C_{OUT1}$ = 22 µF, and $C_{OUT2}$ = 47 µF (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **$\overline{MR}$ Terminal** | | | | | |
| High-level input voltage | | 2 | | | V |
| Low-level input voltage | | | | 0.7 | V |
| Falling edge delay | Measured at $V_O$ | | 140 | | µs |
| Pull-up current source | | | 6 | | µA |

### ELECTRICAL CHARACTERISTICS (continued)

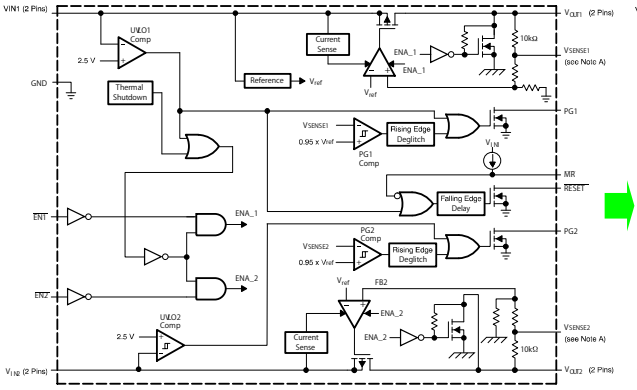
Over recommended operating junction temperature range ($T_J$ = –40°C to +125°C), $V_{IN1}$ or $V_{IN2}$ = $V_{OUT(nom)}$ + 1 V, $I_O$ = 1 mA, $\overline{EN}$ = 0 V, $C_{OUT1}$ = 22 µF, and $C_{OUT2}$ = 47 µF (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **$\overline{MR}$ Terminal** | | | | | |
| High-level input voltage | | 2 | | | V |
| Low-level input voltage | | | | 0.7 | V |
| Pull-up current source | | | 6 | | µA |

## C.4 Pg 7,Fixed Voltage Version

**DEVICE INFORMATION**

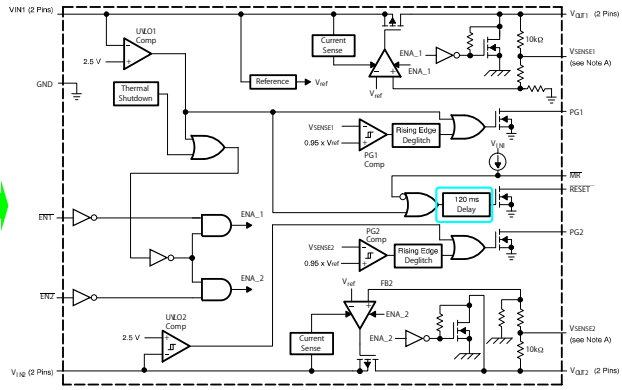
**Fixed Voltage Version**




A. For most applications, $V_{SENSE1}$ and $V_{SENSE2}$ should be externally connected to $V_{OUT1}$ and $V_{OUT2}$, respectively, as close as possible to the device. For other implementations, refer to SENSE terminal connection discussion in the *Application Information* section.

**DEVICE INFORMATION**

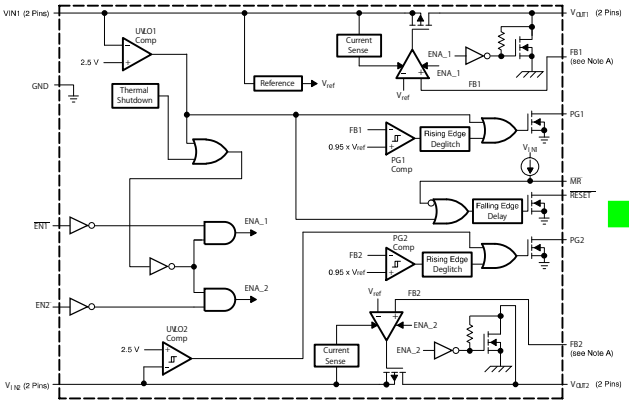
**Fixed Voltage Version**




A. For most applications, $V_{SENSE1}$ and $V_{SENSE2}$ should be externally connected to $V_{OUT1}$ and $V_{OUT2}$, respectively, as close as possible to the device. For other implementations, refer to SENSE terminal connection discussion in the *Application Information* section.

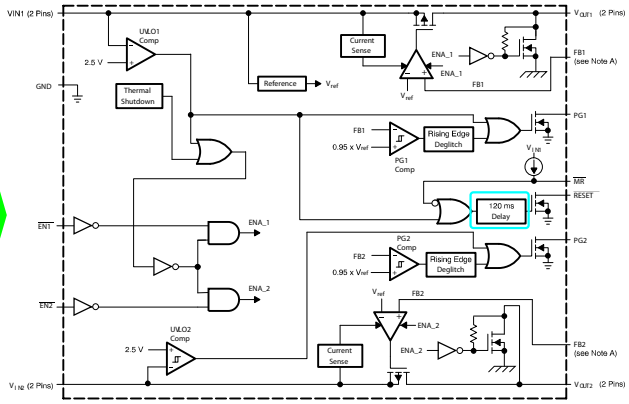
**C.5 Pg 8,Adjustable Voltage Version**

**Adjustable Voltage Version**




A. For most applications, FB1 and FB2 should be externally connected to resistor dividers as close as possible to the device. For other implementations, refer to FB terminals connection discussion in the ***Application Information*** section.

**Adjustable Voltage Version**




A. For most applications, FB1 and FB2 should be externally connected to resistor dividers as close as possible to the device. For other implementations, refer to FB terminals connection discussion in the ***Application Information*** section.

**C.6 Pg 32,REVISION HISTORY**

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| **Changes from Revision D (December, 2007) to Revision E** | **Page** |
|---|---|
| • Corrected pin description for pin 21 in pinout drawing | 1 |
| • Updated *Dissipation Ratings* table values | 4 |
| • Deleted *falling edge delay* specification | 6 |
| • Updated *Fixed Voltage Version* block diagram | 7 |
| • Updated *Adjustable Voltage Version* block diagram | 8 |